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Nonblocking Memory Refresh

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***Abstract*—Since its inception half a century ago, DRAM has required dynamic/active refresh operations that block read requests and decrease performance. We propose refreshing DRAM in the background without stalling read accesses to refreshing memory blocks, similar to the static/background refresh in SRAM. Our proposed Nonblocking Refresh works by refreshing a portion of the data in a memory block at a time and uses redundant data, such as Reed-Solomon codes, in the block to compute the block's refreshing/unreadable data to satisfy read requests. For proof of concept, we apply Nonblocking Refresh to server memory systems, where every memory block already contains redundant data to provide hardware failure protection. In this context, Nonblocking Refresh can utilize server memory system's existing per-block redundant data in the common-case when there are no hardware faults to correct, without requiring any dedicated redundant data of its own. Our evaluations show that on average across five server memory systems with different redundancy and failure protection strengths, Nonblocking Refresh improves performance by 16.2% and 30.3% for 16gb and 32gb DRAM chips, respectively.**

I. Introduction

For half a century, Dynamic Random Access Memory (DRAM) has been the dominant computer main memory. Despite its important role, DRAM has an inherent physical characteristic that contributes to its inferior performance compared to its close relative - SRAM (Static RAM). While DRAM and SRAM are both volatile, DRAM requires dynamic/active refresh operations that stall read requests to refreshing data; in comparison, SRAM relies on latch feedback to perform static/background refresh without stalling any read accesses.

Stalled read requests to DRAM's refreshing data slow down system performance. Prior works have looked at how to reduce the performance impact due to memory refresh [1]–[10]. Some of them have explored intelligent refresh scheduling to block fewer pending read requests [1]–[3]; however, they provide limited effectiveness. As refresh latency increases, many later works have explored how to more aggressively address memory refresh performance overheads by skipping many required memory refresh operations [6]–[10] at the cost of reducing memory security and reliability [11]–[15]; however, this is inadequate for systems that do not wish to sacrifice security and reliability for performance.

To effectively address increasing refresh latency without resorting to skipping refresh, we propose *Nonblocking Refresh* to refresh DRAM without stalling reads to refreshing memory blocks. A memory block refers to the unit of data transferred per memory request. Nonblocking Refresh works by refreshing only some of the data in a memory block at a time and uses redundant data, such as Reed-Solomon code, to compute the inaccessible data in the refreshing block to complete read requests. Compared to the conventional approach of refreshing all the data in a block at a time, Nonblocking Refresh makes up for refreshing only some of the data in a block at a time by operating more frequently in the background. Nonblocking Refresh transforms DRAM to behave like SRAM at the system-level by enabling DRAM to refresh in the background without stalling read requests to refreshing memory blocks.

For proof of concept, we apply Nonblocking Refresh to server memory systems, which value security and reliability. We observe server memory systems already contain redundant data to provide hardware failure protection via an industry-standard server memory feature commonly known as chipkill-correct, which tolerates from bit errors up to dead memory chips [16]–[18]. Because redundant data are budgeted to protect against worst-case hardware failure scenarios, they are often under-utilized when there is minor or no hardware fault. As such, in the context of server memory, we can safely utilize existing under-utilized redundant data to implement Nonblocking Refresh in the common-case, without requiring any dedicated redundant data. Our evaluation shows that across five server memory systems with different failure protection strengths, Nonblocking Refresh improves average performance by 16.2% and 30.3% for 16gb and 32gb DRAM chips, respectively. The performance of memory systems with Nonblocking Refresh is 2.5%, on average, better than systems that only performs 25% of the required refresh.

We make the following contributions in this paper:

- We propose Nonblocking Refresh to avoid stalling accesses to refreshing memory blocks in DRAM.
- We apply Nonblocking Refresh in the context of server memory systems, where existing redundant memory data can be leveraged without increasing storage overhead.
- We find that Nonblocking Refresh improves average performance by 16.2% and 30.3% for server memory systems with 16gb and 32gb DRAM chips, respectively.

The first three co-authors are listed alphabetically by first name.

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II. Background

The lowest-level structure in memory is a cell, which contains one bit of data. Each memory chip consists of billions of cells. Chips accessed in lockstep are referred to as a rank. A rank is the smallest unit that can be addressed in memory commands. When accessing memory, all chips in a rank operate in lockstep to transmit a unit of data called a memory block. Each chip in the rank contributes an equal amount of data to a memory block, usually four or eight bytes; memory chips that access four and eight bytes of data per memory request are referred to as x4 and x8 chips, respectively. Multiple ranks form a memory module, which is commonly referred to as a DIMM (dual in-line memory module). One or more DIMMs form a memory channel. Each channel has a data bus and command bus that are shared by all ranks in the channel (see Figure 1). The processor's memory controller (MC) manages accesses to each channel by broadcasting commands over each channel's command bus.

A. Memory Refresh

A memory cell stores a single bit of data as charge in a capacitor. A cell loses its data if it loses this charge. The charge in a cell may leak or degrade over time; thus, memory refresh is needed to periodically restore the charge held by memory cells. Memory standards dictate that a cell refresh its charge every 64ms [19]. A cell refreshes in lockstep with the other cells in its row. Each chip maintains a counter that determines which rows to refresh.

To refresh a row, a memory chip reads data from a row into its row buffer and then rewrites the data back to the row, thus restoring the charge. Chips refresh multiple rows per refresh interval. The duration of a single refresh interval is called refresh cycle time ($tRFC$). The MC sends a single refresh command to refresh all chips in a rank simultaneously. The duration between refresh commands for one rank is the refresh interval time ($tREFI$). MC can "pull-in" or issue refresh commands earlier than $tREFI$ to allow scheduling flexibility [24]. MC can pull in up to eight refresh commands to reduce the number of refresh commands required later [24].

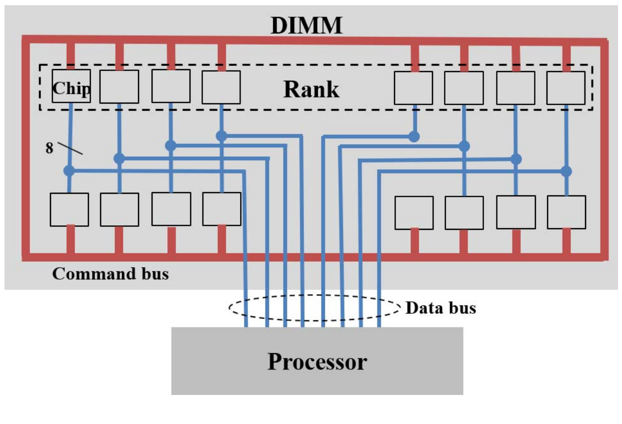


Fig. 1. Memory system layout

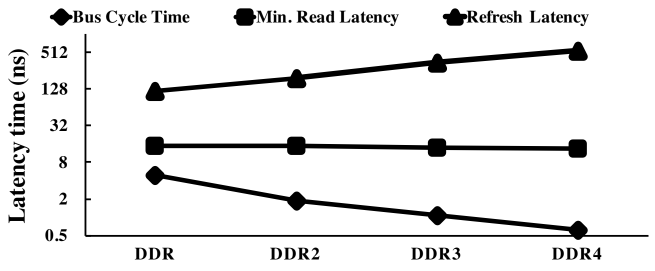


Fig. 2. Historical trends of memory latencies [20]–[23]

Historically, $tRFC$ has increased for every new generation of chips, growing 50% between the last two generations (8gb to 16gb) chips [21]. This increase is attributed to growth of chip density because the time for refresh correlates to the number of rows in memory. In contrast, other memory related latencies have remained steady or decreased across generations. Historical data collected from Micron datasheets, as seen in Figure 2, reveal the improvement of bus cycle time and minimum read latency in comparison with worsening refresh latency [20]. As these trends continue, memory refresh stands out as one of the determining factors in overall memory system performance.

Refreshing chips are unable to service memory requests until their refresh cycle has completed. The inability to access data from refreshing chips stalls program execution. $tRFC$ has been steadily increasing because each new generation of DRAM has higher capacity and, therefore, contains more memory cells to refresh. Using refresh latency from the last four DRAM generations [21], we apply best fit regression to project the refresh latency for the next two generations of memory chips in Figure 3. $tRFC$ will become 880ns and 1200ns in 32gb and 64gb devices, respectively.

B. Skipping Refresh

Many recent works propose skipping many refresh operations, by increasing refresh interval, to improve performance [4]–[10]. For example, RAIDR [5] profiles the charge retention time of DRAM cells in each row in memory and skips refresh operations to memory rows with long retention time.

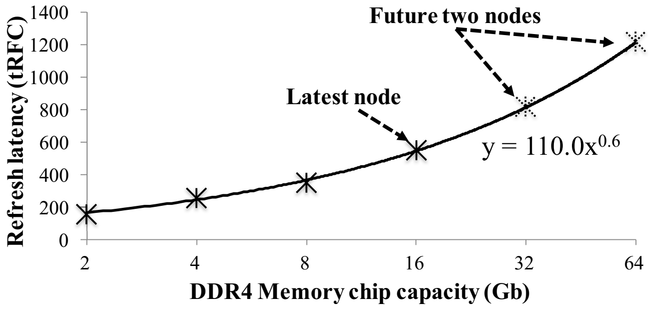


Fig. 3. Historical [21] and projected refresh latency.

However, skipping refresh reduces the average amount of charge stored in DRAM cells and, therefore, significantly increases DRAM vulnerability to read disturb errors [12]. This in turn significantly increases system vulnerability to software attacks that have exploited DRAM read disturb errors [11]–[14]. Operating memory out-of-spec at reduced refresh rate may also increase memory fault rates because retention profiling cannot always identify all weak cells; higher memory fault rate in turn can degrade reliability. Reliability is important for server systems because an hour of server downtime can often lead to millions of dollars loss in revenue [25]. As such, data-center operators and decision-makers are often averse to adopting techniques with unquantifiable reliability risks [26]. Furthermore, out-of-spec operations can also void warranty and system-level agreements and thus degrade serviceability.

In summary, new solutions are needed to address memory refresh performance overheads for systems that have strict security, reliability, and serviceability requirements.

III. Motivation

Because server memory systems often contain many (i.e., 100s to 1000s) memory chips to provide high memory capacity, they need to protect against memory chips failing during system lifetime. As such, every memory block in server systems contains significant redundant data (see Figure 4) for hardware failure protection. The ratio of redundant data to program data in each block ranges from 12.5% to 40.6%.

Refreshing memory chips behave similarly to dead memory chips in that data stored in chips is inaccessible in both cases; as such, it should be possible to reuse the existing redundant data in server memory intended for chip failure protection to also compute data stored in inaccessible refreshing memory chips. To reuse redundant server memory to improve performance, we observe that individual memory chips are highly reliably as evidenced by the fact that systems with few memory chips, such as personal computers, mostly do not provide memory chip failure protection. Because individual chips are highly reliable, only a small fraction of memory locations, on average, experience hardware faults. As such, we can leverage the under-utilized redundant data in common-case fault-free memory locations to implement Nonblocking Refresh.

Figure 5 quantifies the expected fraction of memory pages that have not yet encountered any hardware fault by the N^{th} year of operation.[1] On average across seven years of operations, 97% of memory pages are not affected by any faults. While only a small fraction of memory pages experience fault, server systems protect memory pages with uniform redundant data because chip failures are stochastic events, whose time and location are difficult to predict.

[1]Figure 5 is calculated from the memory chip failure rate and patterns reported in a recent large-scale field study of memory failures [27], assuming eight ranks per channel and 18 chips per rank.

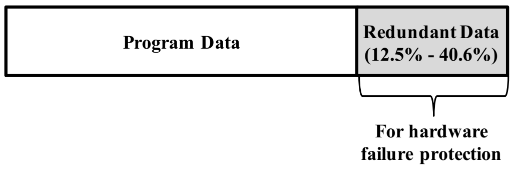

Program Data
Redundant Data (12.5% - 40.6%)
For hardware failure protection

Fig. 4. Composition of a memory block in server memory.

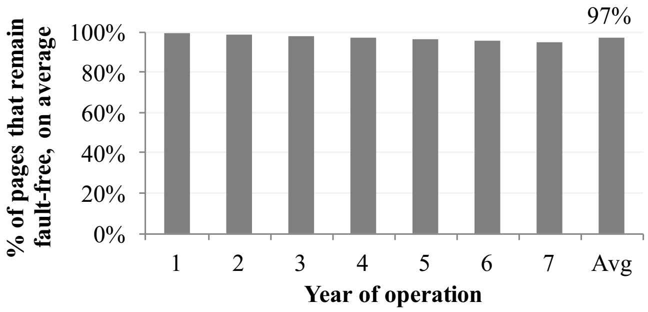


Fig. 5. Expected fraction of memory pages that have not yet been affected by any fault as a function of time.

The general trend in the ratio of redundant data to program data in server memory is also increasing. The JEDEC memory standard reduces data bus width per channel from 64 bits in DDR4 to 32 bits for the upcoming DDR5 [28]. While reducing the width of the data bus naturally reduces the number of data chips per rank, the number of redundant chips per rank used to provide chipkill-correct remains the same; this doubles the ratio of redundant data to program data from 12.5% in a DDR4 rank to 25% in a DDR5 rank. Due to the increasingly disparity between the large amount of redundant data in server memory and the small fraction of that data actually being used to correct errors, we argue redundant data is an underutilized resource that can be reused to also improve memory performance.

IV. Nonblocking Refresh

We propose Nonblocking Refresh to refresh memory blocks while allowing read requests to access the refreshing blocks; it works by refreshing just a portion of the data in a memory block at any point in time, and uses per-block redundant data, such as Reed-Solomon codes, to reconstruct the unreadable/refreshing data in the block to satisfy read requests to the refreshing block. Compared to refreshing an entire block at a time as do conventional blocking refresh, Nonblocking Refresh can make up for refreshing only a portion of data in a block at a time by refreshing more frequently in the background. Nonblocking Refresh transforms DRAM to become functionally similar to SRAM in terms of refresh; under Nonblocking Refresh, DRAM refreshes continuously in the background without blocking read requests to refreshing memory blocks.

In this paper, we focus on exploring Nonblocking Refresh in the context of server memory systems. In this context, Nonblocking Refresh can exploit existing abundant redundant data in server memory to compute refreshing data in each block, without requiring any dedicated redundant data of its own. Designing Nonblocking Refresh for server memory requires addressing three main challenges: 1) How to reuse existing redundant data in server memory to perform Nonblocking Refresh? 2) How to perform the same aggregate amount of refresh as the conventional approach of refreshing an entire block at a time? 3) Redundant data must preserve its original purpose of hardware failure protection in the event that memory faults do suddenly occur. Therefore, a third challenge is how to preserve baseline failure protection while leveraging redundant data to implement Nonblocking Refresh?

A. How to Utilize Existing Redundant Server Memory Data?

Conventional server memory systems cannot exploit redundant data to compute inaccessible data stored in refreshing chips because they refresh all chips in a rank at the same time. As such, all data will be missing from a memory block read from a refreshing rank (see Figure 6A), making it impossible for redundant data to compute any missing data.

To compute inaccessible data stored in refreshing chips, the amount of inaccessible data in each block must be less than the maximum amount of data that the block's redundant data can reconstruct. We propose refreshing few chips in a rank at a time so that only a small fraction of the data in each block are inaccessible due to refresh. Figure 6B shows an example that refreshes only one chip at a time. The MC uses the block's redundant data to compute the missing data in the block to complete the read request to the block.

Computing the missing data is fast because the MC already knows which memory chip(s) are refreshing, unlike regular error correction, where the MC needs to locate the error before computing the error value. Computing the value of errors whose locations are known is called *erasure correction*. The vast majority of latency during error correction is to locate the error; computing the error value after knowing the error location incurs only a few cycles of latency [29]. Erasure correction also only consumes small amount of power. Prior study using 180nm transistor process technology report that erasure correction only consumes 200-500uW [29]; it should be even lower in today's 14nm process technology. Enhancing the MC to perform erasure correction for Nonblocking Refresh also incurs little to no area overhead because the error correction logic in conventional server systems' MCs already contains the hardware to compute the correct values of located errors.

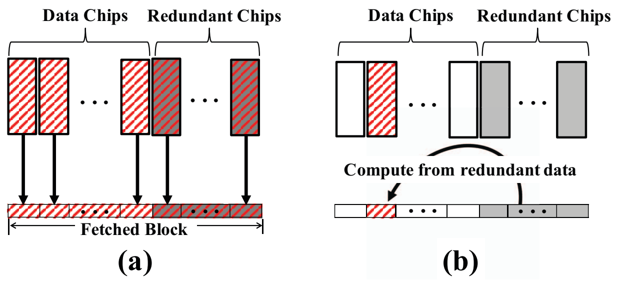


Fig. 6. (a) Conventional refresh. (b) Nonblocking Refresh. Red represents inaccessible data stored in refreshing memory chips.

To enable Nonblocking Refresh, the chips in each rank are logically partitioned into *refresh groups*. A Nonblocking Refresh operation refreshes a single refresh group. Since conventional server memory systems refresh all chips in a rank simultaneously, some hardware modifications are needed to refresh each refresh group individually.

One possible implementation of refresh groups is to refresh the refresh groups in a round-robin fashion and modify each memory chip to ignore refresh commands designated for other refresh groups; modifying a chip to ignore some refresh commands is similar to a recent work that skips refresh [6]. For a rank with N refresh groups, the memory chips belonging to a refresh group ignores $N-1$ out of every N refresh commands such that each command refreshes only one refresh group. By refreshing the refresh groups in a round-robin fashion, the MC can track which refresh group is refreshing by counting the past Nonblocking Refresh operations via a modulo counter. Since current DRAM standards dictate that a refreshing chip should not receive any valid commands, the chips also need to be modified to ignore other commands while refreshing. When a refresh group exits refresh, it may be out-of-sync with the row buffer state of the remaining chips in the rank. The MC can synchronize all chips in the rank by issuing a precharge_all command to the rank.

Another possible implementation of refresh groups is to modify the DIMM rather than the memory chips themselves. We observe that a memory chip ignores all commands, including refresh commands, unless its chip select (CS) input bit is asserted [19]. To refresh individual refresh groups, we can simply devote a CS bit to each refresh group, instead of devoting a CS bit to an entire rank as do conventional systems. The MC initiates Nonblocking Refresh for a refresh group by asserting only the CS bit of the desired refresh group when issuing a refresh command.

B. How to Ensure Each Chip Performs Same Amount of Refresh as Conventional Blocking Refresh

One obvious challenge with refreshing only some of the chips in a rank at a time is how to perform same amount of refresh in each chip as the conventional approach of refreshing all chips in a rank at the same time. The MC must issue Nonblocking Refresh more frequently than conventional blocking refresh to make up for refreshing fewer chips at a time. We observe that because Nonblocking Refresh does not block read requests, the MC can refresh memory continuously in the background with minimum performance impact. Conventional systems with blocking refresh, on the other hand, can only refresh each rank infrequently to avoid excessively blocking read requests. Figure 7 contrasts the timeline of Nonblocking Refresh with the timeline of conventional refresh.

Since Nonblocking Refresh is performed more frequently than conventional blocking refresh, Nonblocking Refresh can incur command bus bandwidth overheads. Assuming a single rank per channel and $tRFC = 550ns$ [21], if the MC issues refresh commands back to back after every tRFC, the aggregate command bus bandwidth is only $0.2-0.4\%$. However, this command bus bandwidth overhead increases proportionally with the number of ranks in the channel; this may translate to non-negligible (e.g., 5%) command bus bandwidth utilization for very large channels. One effective solution for very large channels is to let multiple ranks (e.g., all ranks in the same DIMM) in the same channel perform Nonblocking Refresh in parallel for each refresh command MC places on the command bus.

Depending on the refresh group size and tREFI, Nonblocking Refresh may not always fully keep up the conventional approach of refreshing entire blocks at a time. In this scenario, a memory system with Nonblocking Refresh may need to occasionally perform conventional blocking refresh to meet requirement. Even in this scenario, Nonblocking Refresh still helps to avoid many conventional blocking refresh and, therefore, improves performance compared to only performing conventional refresh. A memory system with Nonblocking Refresh may use a per-rank hardware counter to count the number of past Nonblocking Refresh operations; after a rank has performed the same number of Nonblocking Refresh as there are refresh groups, the MC does not need to issue a blocking refresh to the rank at the next tREFI time interval.

Unlike read requests, write requests can be negatively impacted when each rank refreshes frequently/continuously. Writes to a rank cannot proceed in parallel with refreshing the rank because data in a chip cannot be updated while a chip is refreshing. Write requests still need to wait for a rank to complete any in-flight refresh operations before they can proceed. Therefore, refreshing each rank more frequently can potentially increase write latency and reduce write bandwidth. We note that increasing write latency does not degrade performance because memory writes are not on the critical path of program execution; however, reducing write bandwidth can degrade performance because it can reduce the throughput of memory store instructions.

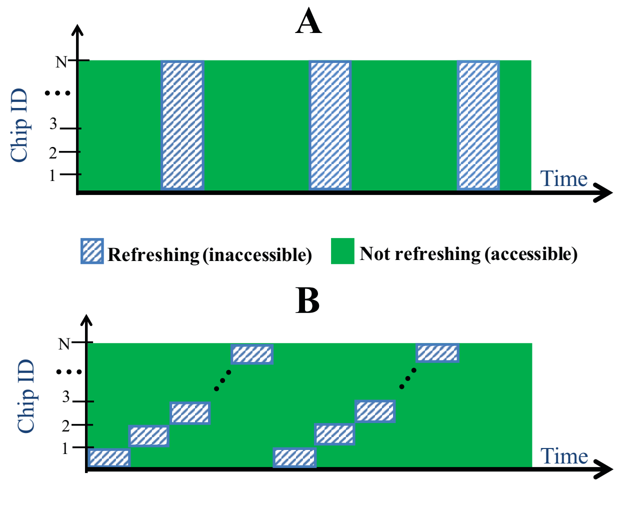


Fig. 7. Timelines of (a) blocking refresh and (b) Nonblocking Refresh

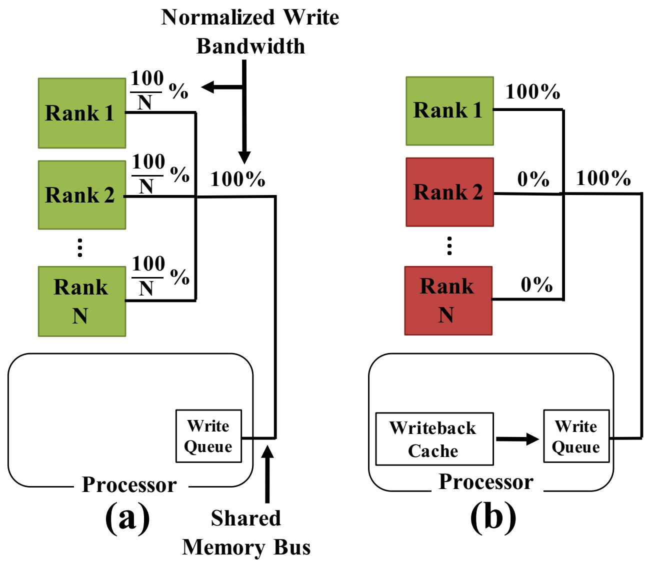


Fig. 8. Write distribution in (a) conventional and (b) proposed memory systems. Green ranks are not refreshing and, therefore, writable; red ranks are refreshing and, therefore, not writable.

To maintain memory write bandwidth while frequently performing Nonblocking Refresh, we make two observations. First, since all ranks in the same channel share the same memory bus, the MC can only write to one rank at a time. Therefore, total write bandwidth in a channel is divided across all the ranks in the channel, as shown in Figure 8A. Second, logically adjacent memory pages are often interleaved across ranks to minimize read latency overheads due to row conflicts. This interleaving causes write requests to distribute fairly evenly among all ranks in the channel. Based on these observations, we propose re-ordering write requests to concentrate each channel's write bandwidth to a few ranks at a time as shown in Figure 8B. This maintains the same channel-level write bandwidth while allowing the remaining ranks in the channel to continuously perform Nonblocking Refresh.

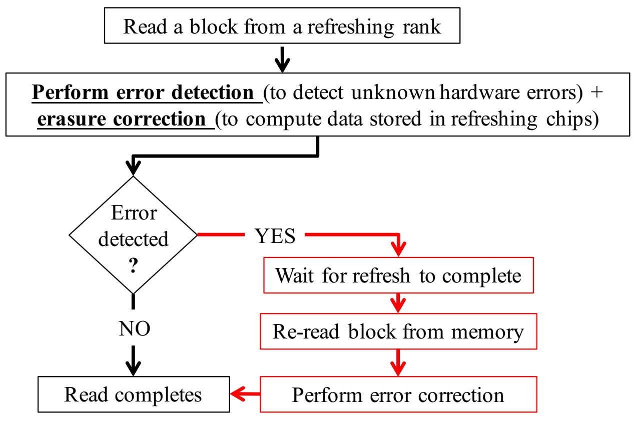
We propose logically grouping the ranks in a channel into separate *write groups*, such that each channel with N ranks contain K write groups, with N/K ranks per write group. During each $tRFC$ interval, the MC writes to one of the K write groups while performing Nonblocking Refresh to the remaining $K-1$ write groups. The remaining ranks will complete their current Nonblocking Refresh after each $tRFC$ interval. At the same time, the MC selects a different write group to write to and again puts the remaining ranks under Nonblocking Refresh. This approach can provide the channel-level write bandwidth of conventional systems while allowing the majority (i.e., $(K-1)/K$) of the ranks to benefit from Nonblocking Refresh. Server memory often contains many ranks per channel to provide adequate capacity; as such, they can often benefit from a large $(K-1)/K$ value (e.g., 3/4 for channels with just four ranks per channel).

Re-ordering write requests to only one write group per $tRFC$ interval requires modifying the MC to buffer more writes. We use Little's Law [30] to estimate the size of the write buffer needed to match the outgoing rate of the write buffer in the worst-case arrival rate of write requests. Little's Law states that the average number of elements in a queue is $L = \lambda \cdot W$, where λ is the average arrival rate and W is the average time each element waits in the queue [30]. In the context of the write buffer, L is buffer size, λ is the memory write bandwidth, and W is how long, on average, a block needs to wait in the buffer until its write group is selected for writes. Assuming write requests account for at most half of total memory requests because a processor typically needs to first fetch a block from memory before writing to the block, λ = 12.8GBps for a 3.2ghz and 64-bit wide channel. With K write groups, a newly arrived block waits, on average, $K \cdot tRFC$ before its write group is selected; as such, we pessimistically estimate $W = K \cdot tRFC$. $W = 4 \cdot 550 = 2200ns$ assuming a server system with 16gb chips (550ns $tRFC$) [21] and four write groups per channel. Together, the new size of the write buffer for the channel should be $L = 12.8 \cdot 2200 =$ 28kB.

We implement the write buffer as a set-associative writeback cache. When the MC receives an evicted dirty block, the MC places the block in the writeback cache instead of immediately placing it in the write queue used by the memory command scheduler. At the end of each $tRFC$ interval, the MC selects an active write group to write to for the next $tRFC$ interval; the MC first determines the most occupied set in the writeback cache and then selects the write group with the most cachelines in that set as the active write group. However, there are two special cases. If the most occupied set in the writeback cache has less than a threshold occupancy (e.g., 75% in our evaluation), the MC does not select an active write group so that all write groups can continue to perform Nonblocking Refresh during the next $tRFC$ interval. On the other hand, $tREFI$ may not be evenly divisible by $tRFC$; if a blocking refresh is required at the next $tREFI$ interval and there is not enough time for perform a Nonblocking Refresh, all ranks become active write groups. After selecting one or more active write groups, the MC drains the write group(s)' dirty blocks from the writeback cache to the write queue whenever it has available entries, starting from the most occupied cache set to the adjacent set in a round-robin fashion. The memory command scheduler only scans the write queue to schedule write commands; it is oblivious of the writeback cache.

C. How to Preserve Failure Protection?

Nonblocking Refresh improves system performance by reusing the redundant data in server memory to compute the inaccessible data in refreshing memory chips. This should not detract from the original purpose of redundant data - hardware failure protection. The following lists a set of sufficient conditions that, if all true, enables a server memory system with Nonblocking Refresh provide equal hardware failure protection as a conventional system with same amount of redundant data: A) Memory systems with Nonblocking Refresh should not increase the physical/raw fault rate of



Read a block from a refreshing rank
Perform error detection (to detect unknown hardware errors) +
erasure correction (to compute data stored in refreshing chips)
Error detected ?
YES
NO
Wait for refresh to complete
Re-read block from memory
Perform error correction
Read completes

Fig. 9. Action flow for reading from a rank under Nonblocking Refresh.

memory chips compared to conventional systems. B) Both systems should have identical error *detection* strength. C) Both systems should have identical error *correction* strength.

We meet A) because memory systems with Nonblocking Refresh can perform the same amount of refresh as conventional memory systems (see Section IV-B) and, therefore, can maintain baseline memory system's physical fault rates. To meet B), we observe that each block contains some redundant data for error detection; as such, we can meet B) by using the same amount of redundant data to detect fault-induced random errors for each read request as baseline memory systems. To meet C), only when no random errors are detected does Nonblocking Refresh opportunistically reuse the redundant data intended for error correction to compute data missing due to refresh. When random errors are detected in a fetched block, the MC waits for the rank to finish its in-flight refresh and then re-read the same block from memory, as shown in Figure 9. Since the rank is no longer refreshing when the second read is performed, the re-fetched block no longer misses any of its data due to refresh; as such, the redundant data in the re-fetched block can correct fault-induced random errors in the exact same way as baseline memory system and, therefore, preserve baseline error correction strength. We examine three specific server memory systems to further demonstrate how to meet B) and C) in more detail.

Many Intel and AMD server systems protect memory with single chipkill-correct (SCC) [16], [31]. SCC memory systems guarantee detection and correction of one faulty chip per rank. SCC memory systems protect K data bytes, each from a different data chip in a rank, with two check bytes, each from a different redundant chip in a rank. We observe that the same check bytes in a codeword can be used in many different ways [32]. R check bytes can guarantee detection and correction of R/2 unknown error bytes; as such, the two check bytes per codeword in SCC memory systems can guarantee detection and correction of one random error byte. Meanwhile, the same R check bytes can also be used instead to guarantee detection of Q unknown error bytes and correct another P erasures (i.e., missing bytes at a known locations), where

$P + Q = R$ [32]. When applying Nonblocking Refresh to SCC memory systems, the refresh group size should be one; as such, MC only uses $P = 1$ check byte per codeword for erasure correction. Since there are two check bytes per codeword in SSC memory systems, each codeword can still guarantee detection of $Q = 2 - 1 = 1$ unknown error byte per codeword and, therefore, guarantee single chip failure detection just like baseline SSC systems that only perform conventional blocking refresh. Figure 10A shows a detailed example for SCC memory systems where the third data chip in a rank is being refreshed. Figure 10B shows a corresponding codeword read from the refreshing rank; the third byte in the codeword is missing because the third chip in the rank is refreshing. The MC can use any one of the codeword's two check bytes to compute the missing byte via erasure correction; the remaining check byte can guarantee detection of any single random error byte in the codeword and, therefore, guarantee detection of one chip failure.

Many IBM servers provide MCC in their memory systems to correct multiple faulty chips per rank as long as a second chip does not fail before the first faulty chip has been logically replaced [17]. Under MCC, each rank has four redundant chips, two used in the same manner as SCC to guarantee single-chip failure detection and two spare chips to logically replace up to two previously observed faulty data chips [17]. When applying Nonblocking Refresh, a MCC memory system can modify each codeword to store four check bytes, instead of two check bytes and two spare data bytes. With four check bytes per codeword, a MCC memory system can use one check byte per codeword to guarantee single-chip failure detection at the rank level and the remaining three check bytes per codeword to implement a refresh group size of three. In the uncommon-case when a MCC memory system needs to replace a faulty data chip, it can revert the faulty rank back to storing two check bytes and two spare bytes per codeword.

High-end IBM servers protect their memory systems with RAIM to tolerate the complete failure of an entire DIMM [33]. A RAIM memory system contains 45 chips per rank, organized in groups of $45/5 = 9$ chips across five different DIMMs, as shown in Figure IV-C. Four of the groups store data; the fifth group stores a bitwise parity of the four data groups to provide error correction. Each data group also contains one redundant chip to store CRC guarantee detection of a single chip failure per data group. When applying Nonblocking Refresh, the refresh group size is nine. Eight check bytes from the parity group can compute the program data missing due to Nonblocking Refresh, while the 9th check byte from the parity group can compute the error detection byte for the eight computed data bytes to guarantee the same single chip failure detection as a conventional RAIM system. When the parity group itself is refreshing, the MC does not need to reconstruct any data for fetched blocks because no program data are missing from these blocks when only the parity group is refreshing.

One potential performance bottleneck with opportunistically reusing existing redundant data intended for hardware failure protection to implement Nonblocking Refresh is that requiring a second read whenever an error is detected can effectively increase error correction latency to $tRFC$. If a rank experiences a permanent chip failure, every read to the require will require error correction. To address this problem, the MC can dynamically decide to only perform conventional blocking refresh for faulty ranks. We will quantify the performance impact of permanent chip faults in Section VI.

V. Methodology

A. *Baselines*

We evaluate a conventional memory refresh baseline that refreshes each rank every tREFI time interval; we refer to this baseline as *Conventional Refresh*. We also evaluate a baseline that completely skips 75% of refresh operations and optimistically assume that it requires no other operations or overheads; this baseline represents the best-case of all prior works that propose skipping refresh [6]–[10]. We refer to this baseline as *Skipping Refresh*.

B. *Processor and Workloads*

We simulate a 16-core out-of-order processor using Gem5 [34], a cycle-accurate micro-architectural simulator. Table I lists the micro-architectural parameters used for simulation.

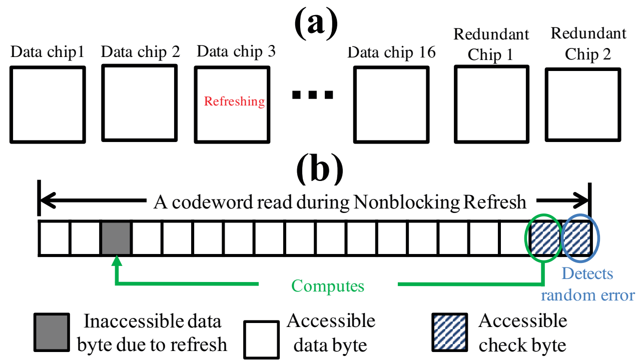


Fig. 10. (a) A SSC memory rank under Nonblocking Refresh. (b) a codeword read from the refreshing rank.

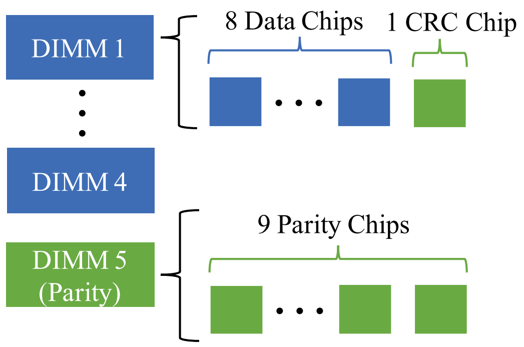


Fig. 11. Layout of a rank with RAIM protection.

TABLE I
PROCESSOR MICROARCHITECTURE

Core	16 cores, 3GHz, 4-issue OOO 128 ROB entries, 64B cacheline size
L1 d-cache, i-cache	2-way, 64kB, 1 cycle
Private L2 cache	8-way, 512kB, 3 cycles
Shared L3 cache	32-way, 32MB, 14 cycles

TABLE II
MIXED WORKLOAD COMPOSITION

mixA	4 omnetpp, 4 mcf, 4 wrf, 4T ocean_cp
mixB	4 bwaves, 4 cactusADM, 4 wrf, 4T ocean_cp
mixC	4 sjeng, 4 cactusADM, 4 radiosity, 4T radix
mixD	4 mcf, 4 GemsFDTD, 4T barnes, 4T radiosity
mixE	4 cactusADM, 4 bwaves,4 sjeng, 4T fft
mixF	4 mcf, 4 omnetpp,4 astar, 4T fft
mixG	4 GemsFDTD,4 astar, 4 bwaves, 4T barnes

We obtain cache access latencies from CACTI for the 32nm technology node [35]. We evaluate 16 threads per workload, seven single-application NASBench [36] workloads and seven multi-programmed workloads (see Table II for composition); only native and reference inputs are used. The workloads' memory footprints range from 10GB to 35GB and are 17GB on average. We fast forward each workload until all multi-threaded application(s) have initialized and then by another 20 simulated seconds. Next, we warm up the caches by 20 simulated milliseconds and then perform cycle-accurate simulation for the next 10 milliseconds. Since all workloads contain multi-threaded applications, we measure throughput not by total instructions, but by FLOPs for workloads with only FP benchmarks and by instructions that access main memory for the remaining workloads. Figure 12 characterizes the memory behavior of these workloads during the 10 millisecond cycle-accurate measurement.

C. Memory System Modeling

We use Ramulator [37] and DRAMPower [38] to measure memory performance and power, respectively, for 3200Mhz DDR4 DRAM by using the latency and current values reported in [21] as input parameters. We model the $tRFC$ of the latest 16gb chips and the future 32gb chips by using the values given in Figure 3. When modeling the future 32gb chips, we pessimistically assume latencies unrelated to refresh remain the same as current DRAMs, instead of keep reducing according to historical trends as shown in Figure 2. We

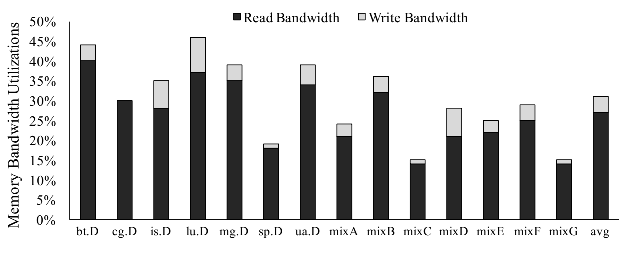


Fig. 12. Workload characterization.

TABLE III
EVALUATED MEMORY CONFIGURATIONS

System	Chip Width	Chips/rank	Channels	Redundant chips
SCC_X4	X4	18	four	two (12.5%)
SCC_X8	X8	10	four	two (25%)
MCC_X4	X4	36	two	four (12.5%)
MCC_X8	X8	20	two	four (25%)
RAIM	X4	45	two	twelve (40.6%)

simulate the FR-FCFS scheduling policy and the open-page row buffer policy and prioritize reads over writes. We evaluate an address mapping policy that interleaves logically adjacent pages across channels, banks, and then ranks. We evaluate four ranks per channel. Each channel contains a 64-entry read queue, 64-entry write queue, and 64-entry command queue. For Nonblocking Refresh, we model a 36-way 36KB writeback cache per 64-bit channel and four write groups per channel, where each rank is a write group. For the baselines, we model staggered refresh, similar to prior works [1], [6], and optimize staggered refresh by applying DARP [1] at the rank level.

We evaluate the three memory systems described in Section IV-C - SCC, MCC, and RAIM memory systems. Commercial SCC memory systems and MCC memory systems use X4 and X8 memory chips, respectively [16], [17]; we refer to them as SCC_X4 and MCC_X8. To explore the effectiveness of Nonblocking Refresh when applied to server memory systems with different redundancy, we also evaluate SCC and MCC implementations using X8 and X4 memory chips, respectively; we refer to these implementations as SCC_X8 and MCC_X4, respectively. We implement SCC_X8 by cutting the number of chips per rank in MCC_X8 by half; we implement MCC_X4 by replacing all the chips in MCC_X8 with X4 chips and doubling the number of data chips per rank. Table III summarizes the memory organization for the evaluated memory systems.

When modeling Nonblocking Refresh, we set refresh group size to one for SCC_X4 and SCC_X8. We set refresh group size to nine for RAIM memory systems. For MCC_X8 memory systems, there are six refresh groups with three chips and one refresh group with two chips because each rank contains 20 chips, which is not divisible by three. We set refresh group size to three for MCC_X4 memory systems. We model the latency of erasure correction as four clock cycles; this corresponds to the latency of the Forney algorithm, which computes the correct values of located errors [29].

VI. EVALUATION

A. Performance Comparison

Figure 13 shows the average performance improvement of Nonblocking Refresh over Conventional Refresh for 16gb and 32gb DRAM. Each bar (e.g., the bar for "SCC_X4") in Figure 13 shows the average performance improvement across all 14 workloads when Nonblocking Refresh and Conventional Refresh are applied to the same memory system (e.g., "SCC_X4"). On average across the five memory systems, Nonblocking Refresh provides 16.2% and 30.3% performance

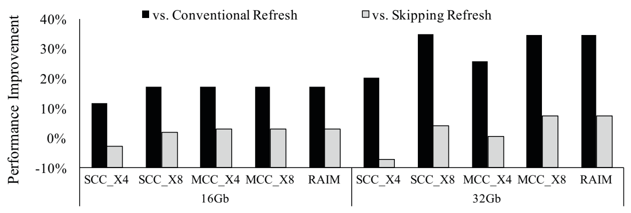


Fig. 13. Average performance improvement vs. Conventional Refresh and Skipping Refresh for 16gb and 32gb DRAM.

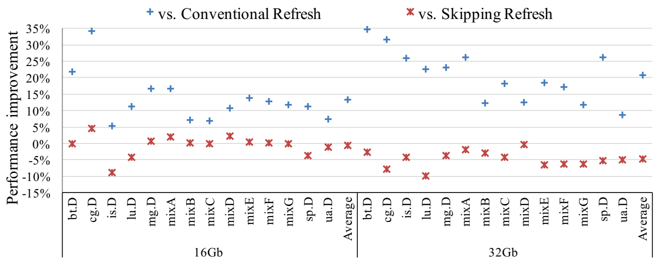


Fig. 15. Performance improvement for SCC_X4 memory systems.

improvement for 16gb and 32gb DRAM, respectively. The performance improvement is higher for 32gb DRAM because 32gb DRAM has a longer refresh latency than 16gb DRAM; when refresh latency is longer, reducing the performance overhead of memory refresh can yield greater overall system-level performance benefit.

SCC_X4 memory systems receive the least performance improvement; it is only 13% for 16gb DRAM and 21.0% for 32gb DRAM. In comparison, the average performance improvement obtained under the remaining memory systems are $16.9\% - 17.1\%$ for 16gb DRAM and $27\% - 35\%$ for 32gb DRAM. SCC_X4 memory systems receive the least performance benefit because Nonblocking Refresh can only refresh $1/18^{th}$ of each rank at a time, the lowest among all five memory systems. As a result, SCC_X4 memory systems with Nonblocking Refresh must perform the most blocking refresh operations among all evaluated memory systems.

Figure 13 also shows the average performance improvement of Nonblocking Refresh over Skipping Refresh for 16gb and 32gb DRAM. On average across the five memory systems, Nonblocking Refresh provides 2.3% and 3% performance improvements compared to Skipping Refresh for 16gb and 32gb DRAM, respectively. Nonblocking Refresh can sometimes perform better than Skipping Refresh because Skipping Refresh still requires performing some blocking refresh; on the other hand, when Nonblocking Refresh can completely keep up with blocking refresh, *all* blocking refreshes can be prevented. More memory systems show performance improvement relative to Skipping Refresh under 16gb DRAM chips than under 32gb DRAM chips because 16gb chips have shorter refresh latency, which enables Nonblocking Refresh to more easily keep up with blocking/full-rank refresh. Note that while the performance of Nonblocking Refresh is within 3%, on average, of Skipping Refresh, Nonblocking Refresh meets the required amount of refresh and, therefore, is applicable to systems with strict security and reliability requirements.

Figure 15 shows that Nonblocking Refresh consistently provides higher performance than conventional refresh for all the workloads with a MCC_X8 memory system. $cg.D$ enjoys the highest performance improvement - 28% and 51% - for 16gb and 32gb DRAM, respectively. Figure 14 shows both memory-intensive workloads such as $bt.D$ and $lu.D$ (see Figure 12) and workloads with low bandwidth utilization, such as $mixC$ and $mixG$, can benefit from Nonblocking Refresh; workloads with low bandwidth utilization also benefit from reducing blocking refreshes because the long refresh latency of $> 500ns$ can still stall execution for a long time even if memory accesses are less frequent. Figure 14 shows the performance improvement of Nonblocking Refresh for a SCC_X4 memory system follows similar trends.

B. Power Comparison

Figure 16 shows the power consumption of memory systems with Nonblocking Refresh normalized to memory systems with conventional blocking refresh and Skipping Refresh. The power consumption of memory systems with Nonblocking Refresh is higher than memory systems with conventional refresh. This is because Nonblocking Refresh improves performance compared to conventional refresh; as such, memory systems with Nonblocking Refresh can complete more read requests and, therefore, consume more power. For this reason, Figure 16 shows that the power increase for systems which gain the least performance benefit from Nonblocking Refresh, such as SCC_X4, is lower than that of systems which gain the most performance benefit from Nonblocking Refresh, such as RAIM and MCC_X8. Note that while Nonblocking Refresh improves

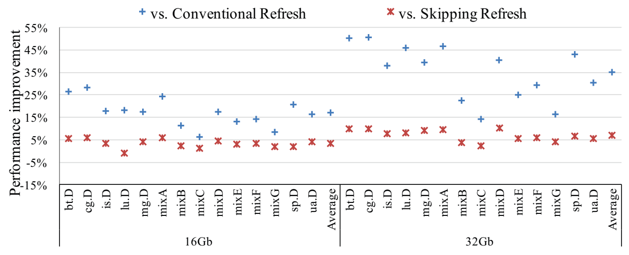


Fig. 14. Performance improvement for MCC_X8 memory systems.

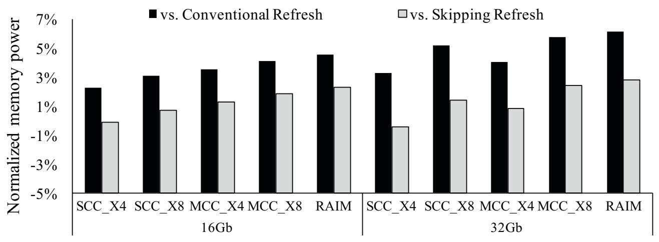


Fig. 16. Memory power vs. Conventional Refresh and Skipping Refresh.

performance by 17% to 35%, it increases memory power consumption by only 2% to 6%; this is because Nonblocking Refresh reduces the average power consumption of memory read requests since they are ignored by refreshing chips in a rank when the rank is performing Nonblocking Refresh.

C. Performance Analysis for Faulty Ranks

To quantify the effects of permanent chip failure on Nonblocking Refresh, we evaluate the performance degradation when a rank falls back on performing only conventional blocking refresh. Figure 17 shows the performance of Nonblocking Refresh for each memory configuration when one, two, or three ranks out of the four ranks per channel only perform conventional blocking refresh; this is normalized to the performance of a memory system where all four ranks are performing Nonblocking Refresh. The presence of faulty ranks impacts the performance of memory systems with 32gb DRAM more than memory systems with 16gb DRAM because the longer refresh latency in the former impacts system performance more than the latter; as such, memory systems with 32gb DRAM have more to lose when some of their ranks cannot perform Nonblocking Refresh.

To estimate the average performance degradation due to chip failures, we assume that a rank falls back on performing only conventional blocking refresh after encountering a single permanent multi-bank or multi-rank fault [27]; the memory system retires all pages affected by smaller faults, such as permanent bank, column, or row faults, because each such fault affects only $0.4\%-0.8\%$ of each evaluated system's total memory capacity. Assuming the above and the memory chip fault rates reported in [27], each rank falls back on performing only conventional blocking refresh $< 1\%$ of the time, on average across a seven-year lifetime.

D. Writeback Cache Size Sensitivity Analysis

The writeback cache is an important component of Nonblocking Refresh. To evaluate how the writeback cache size can affect Nonblocking Refresh performance, we measure the performance of Nonblocking Refresh with increased and decreased writeback cache sizes. Figure 18 shows the performance of Nonblocking Refresh in SCC_X4 memory systems with a smaller, 36-Way 2KB per channel writeback cache and with a larger, 36-Way 72 KB per channel writeback cache; this is normalized to the performance of Nonblocking Refresh in a SCC_X4 memory system using 32gb DRAMs with the proposed 36-Way 32KB per channel writeback cache. Our evaluation shows that Nonblocking Refresh performance does not benefit from a bigger 72KB writeback cache; this is because a 36KB writeback cache is already large enough to maintain the same write bandwidth for Nonblocking Refresh as conventional systems. On the other hand, an insufficient writeback cache size causes a significant degradation in Nonblocking Refresh performance. For workloads such as $lu.D$ and $mixD$, which have high write bandwidth utilization (see Figure 12), using a small 2KB writeback cache can degrade performance by almost 40%.

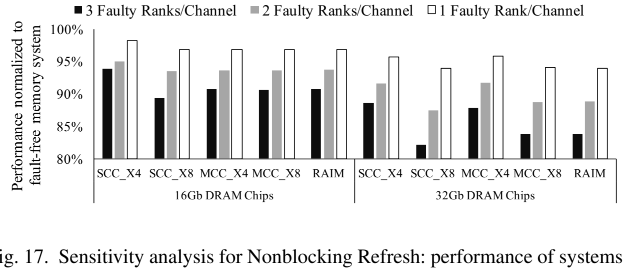


Fig. 17. Sensitivity analysis for Nonblocking Refresh: performance of systems with faulty chips normalized to performance of fault-free systems.

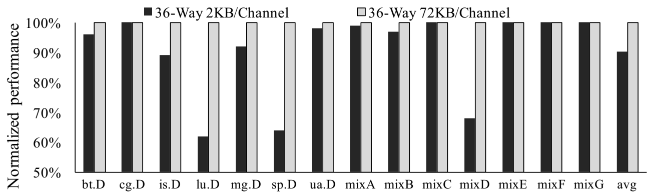


Fig. 18. Performance of Nonblocking Refresh with different writeback cache sizes normalized to 32KB writeback cache.

VII. Related Works

A. Other Works that Leverage Redundant Data

To enable future DRAM density scaling, memory manufacturers may embed error correcting code (ECC) bits and ECC logic within future memory chips [39], [40]; this is known as *on-die ECC*. In the context of DDRx server memory, on-die ECC has been proposed to correct bit errors due to manufacturing defects in future DRAMs [39], [40]; one can envision a strong-enough (and expensive-enough) on-die ECC implementation that also reduces the refresh rate of future DRAMs by correcting errors in DRAM cells with lower retention time than average. However, how much refresh rate can be reduced is limited by the mean/median retention time, which keeps reducing as DRAM cell size reduces. As such, Nonblocking Refresh, which can directly tackle the performance overheads of high-rate refresh head on without reducing refresh rate, provides orthogonal/additive performance benefits/scaling beyond techniques that do require reducing DRAM refresh rate to improve memory performance.

Erasure coding has been used in other contexts to compute data in temporarily inaccessible storage or memory devices. For example, BitTorrent, a popular peer-to-peer file sharing network, creates redundant file chunks using erasure codes to enable clients to compute inaccessible file chunks stored in temporarily off-line peers from redundant file chunks distributed across the network [41]. Shibo et al. [42] propose adding redundant HMCs (Hybrid Memory Cubes) storing erasure codes to compute the data stored in HMCs currently placed in inaccessible power-down modes. Yan et al. [43] propose using erasure coding to compute data in Flash chips that are occupied by on-going garbage collection operations. Mohammad et al. [44] propose adding redundant PCM (Phase Change Memory) chips to store erasure codes to compute inaccessible data stored in PCM chips occupied by long latency writes. However, we apply erasure codes in the context of DRAM refresh and address many new challenges specific to this new application context.

B. Fine-Grained Refresh

Other works have proposed leveraging fine-grained control of refresh scheduling to enhance parallelization of refresh and access to DRAM. Alternative refresh modes that operate at a finer granularity than traditional refresh break each refresh operation into smaller units. Although this offers some performance benefits by reducing the size of inaccessible memory region in each refresh cycle, access to a refreshing block still stalls; as such, fine-grained refresh is a stopgap solution that do not scale well in the face of growing DRAM density.

One type of fine-grained refresh is per-row refresh, which refreshes one row every refresh command. This requires significantly more refresh commands than traditional refresh, leading to increased consumption of command bus bandwidth. Support for per-row refresh in standard DRAM has been deprecated due to its high command bus overhead.

DDR4 DRAM includes a Fine Granularity Refresh (FGR) feature with 2x and 4x refresh modes as an alternative to traditional 1x mode. By refreshing fewer rows per command than 1x mode, 2x and 4x refresh modes have a shorter $tRFC$ at the cost of issuing commands twice and four times more frequently, respectively. The success of FGR is limited because $tRFC$ does not decrease proportionally with increasing refresh rate. More specifically in a 16gb DDR4 system, 2x mode takes almost 30% longer than 1x mode refresh the same number of rows [19]. Due to this overhead, previous works have found that FGR offer small performance benefits [2].

VIII. Generality of Nonblocking Refresh

While we apply Nonblocking Refresh in the context of server memory systems, Nonblocking Refresh is applicable to DRAM-based memory systems in general. For example, desktop/laptop memory systems use the same rank architecture as server memory systems; therefore, they can perform Nonblocking Refresh by adding a redundant chip to the rank and then use the same Nonblocking Refresh implementation as we described for server memory systems.

Nonblocking Refresh is also applicable to memory systems that access only one DRAM chip per memory request, such as High Bandwidth Memory (HBM) and smartphone memory (i.e., LPDDRX DRAM), because the internal organization with each DRAM die mirrors a memory channel's organization. Consider HBM for example. There are multiple banks sharing a common data bus in each DRAM die [45], just like there are multiple ranks in a channel sharing a common data bus. There are also multiple sub-arrays per bank just like there multiple chips per rank [45]. In addition, each memory block is spread across multiple sub-arrays in one bank of a DRAM die, just like how a memory block is spread across a rank [45]. As such, HBM devices can implement Nonblocking Refresh by refreshing a portion of the sub-arrays in a bank at a time and adding redundant sub-arrays to each bank to compute the inaccessible data in refreshing sub-arrays.

In addition to improving raw system performance, avoiding read stalls due to DRAM refresh also reduces performance variability. Performance variability is a major concern for real-time systems because it complicates task scheduling. Conventional blocking DRAM refresh introduces a significant source of performance variability for real-time systems [46], [47]. As such, applying Nonblocking Refresh to the memory systems of real-time systems also provides an added benefit of simplifying task scheduling.

IX. Conclusion

Modern DRAM requires increasingly frequent refresh operations that block memory read requests and, therefore, slow down system performance. To effectively tackle the increasing performance overhead of memory refresh, many prior works have proposed skipping refresh operations; however, this can reduce security and reliability. A new solution is needed for systems with strict security and reliability requirements.

To effectively address increasing refresh latency without resorting to skipping refresh, we propose *Nonblocking Refresh* to refresh DRAM without stalling reads to refreshing memory blocks. Nonblocking Refresh works by refreshing only some of the data in a memory block at a time and uses redundant data, such as Reed-Solomon code, to compute the inaccessible data in the refreshing block to complete read requests. Compared to the conventional approach of refreshing all the data in a block at a time, Nonblocking Refresh makes up for refreshing only some of the data in a block at a time by operating more frequently in the background. Nonblocking Refresh transforms DRAM to behave like SRAM at the system-level by enabling DRAM to refresh in the background without stalling read requests to refreshing memory blocks.

For proof of concept, we apply Nonblocking Refresh to server memory systems, which value security and reliability. We observe that modern server memory systems contain redundant data to recover from memory chip failures; because this redundant data is budgeted for the worst-case memory hardware failure scenarios, a large fraction of the redundant data is not being used in the common case when there are no/little hardware errors to correct. As such, we propose utilizing the under-utilized redundant data in server memory systems to compute the inaccessible data stored in refreshing chips. Our evaluations show that on average across five server memory systems with hardware failure protection strengths, Nonblocking Refresh improves performance by 16.2% and 30.3% for 16gb and 32gb DRAM chips, respectively.

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