

# IODA: A Host/Device Co-Design for Strong Predictability Contract on Modern Flash Storage

Huaicheng Li<sup>☆☆</sup>, Martin L. Putra<sup>☆</sup>, Ronald Shi<sup>☆</sup>,  
Xing Lin<sup>\*</sup>, Gregory R. Ganger<sup>\*</sup>, Haryadi S. Gunawi<sup>☆</sup>

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<sup>☆</sup>University of Chicago, <sup>\*</sup>Carnegie Mellon University, <sup>\*</sup>NetApp

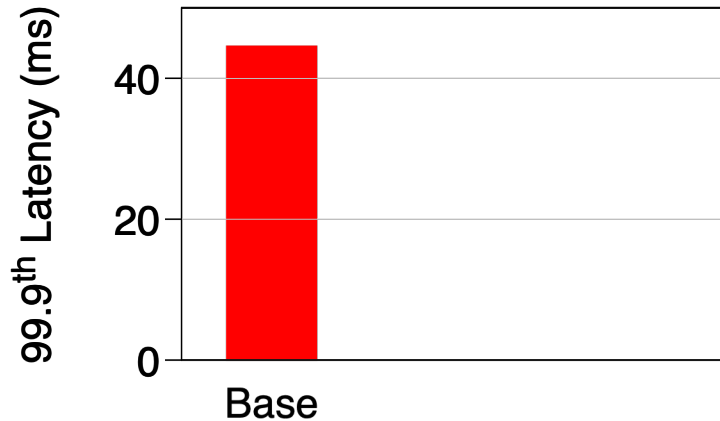
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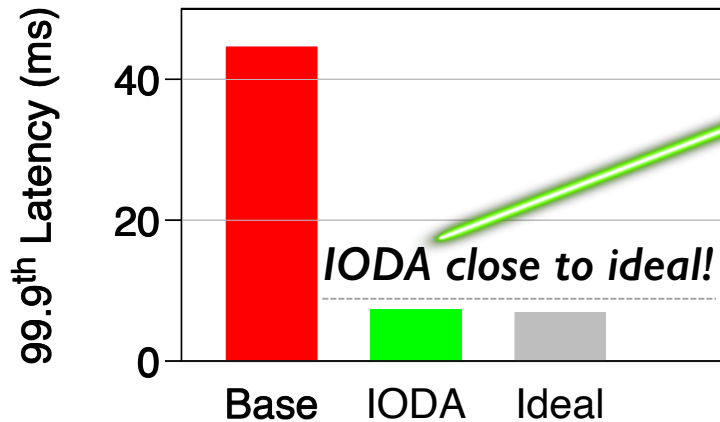
*“Small but powerful”*

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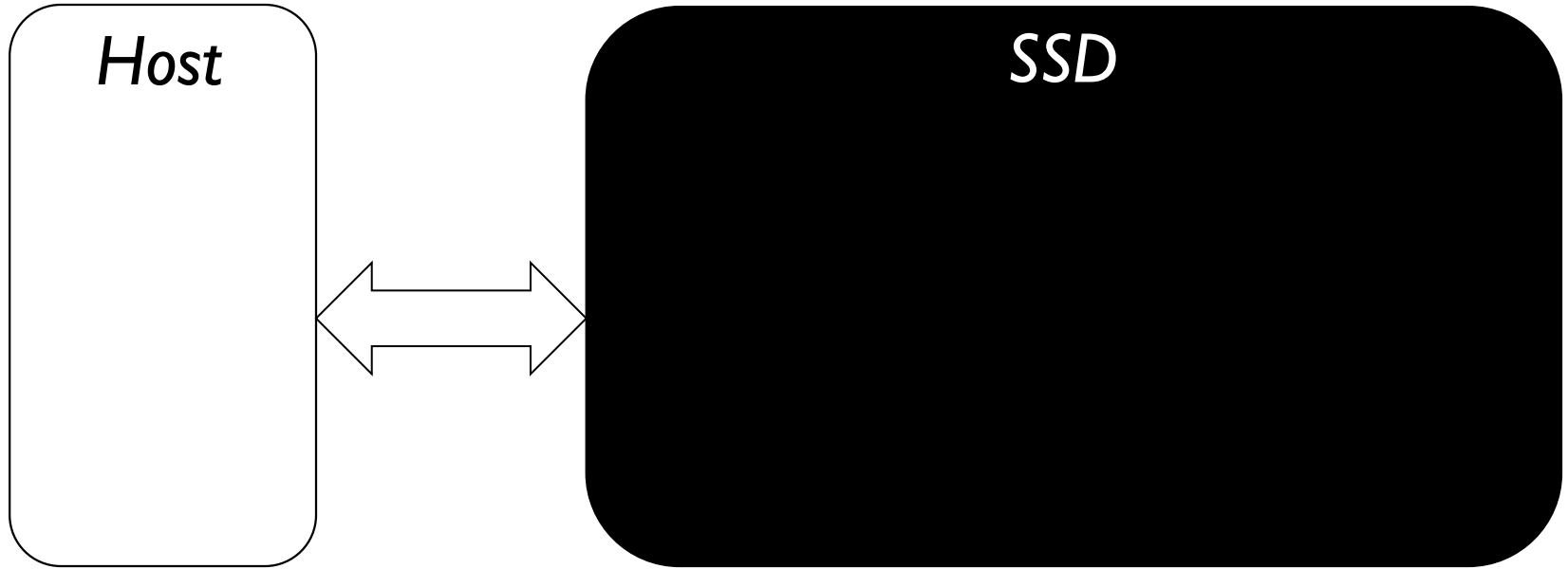
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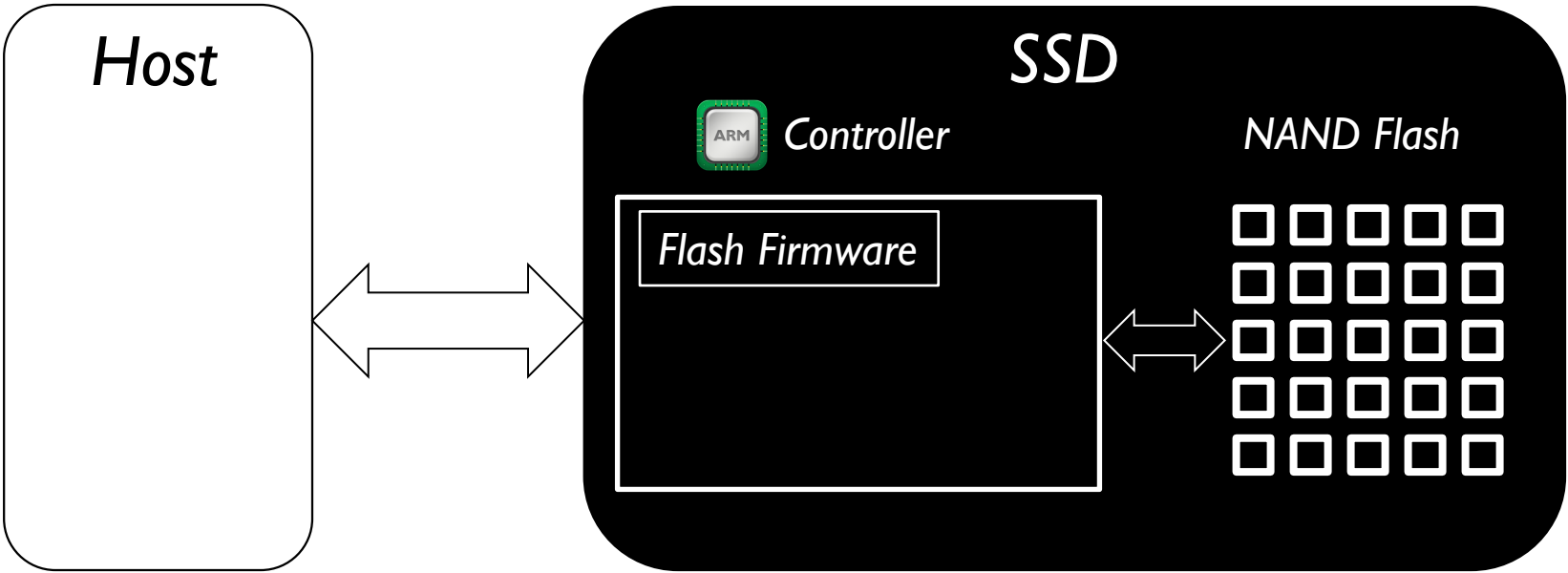


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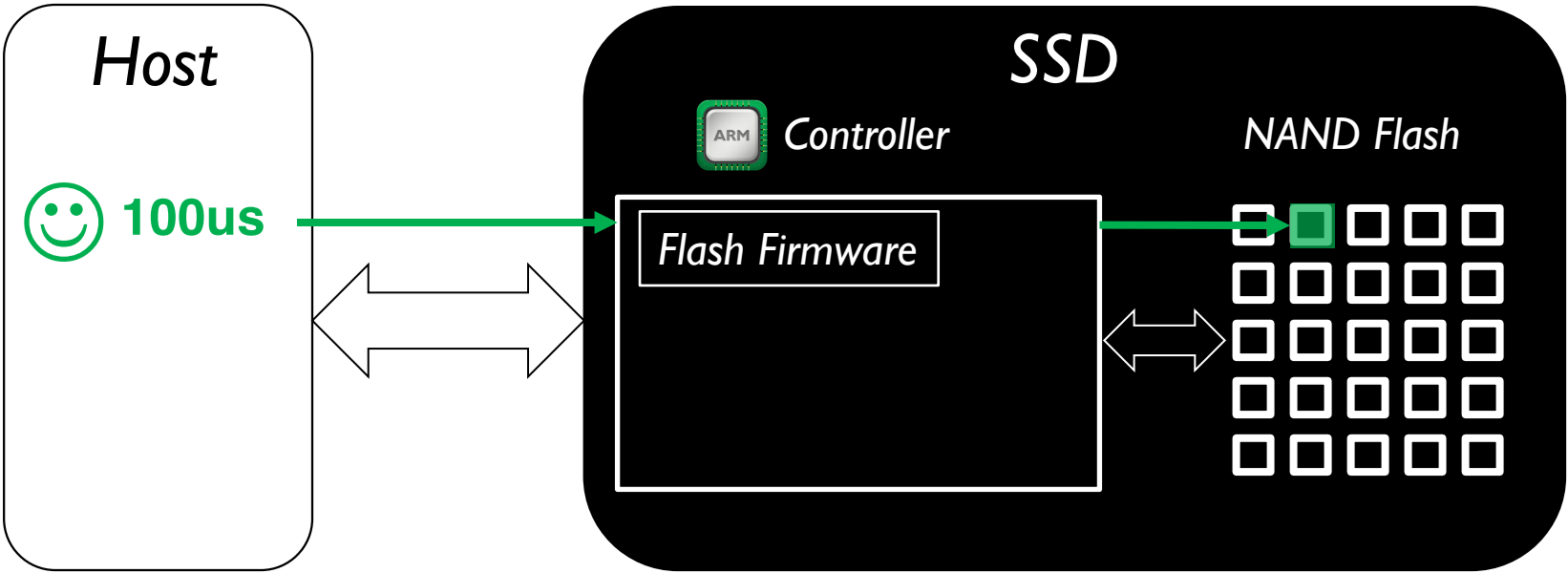
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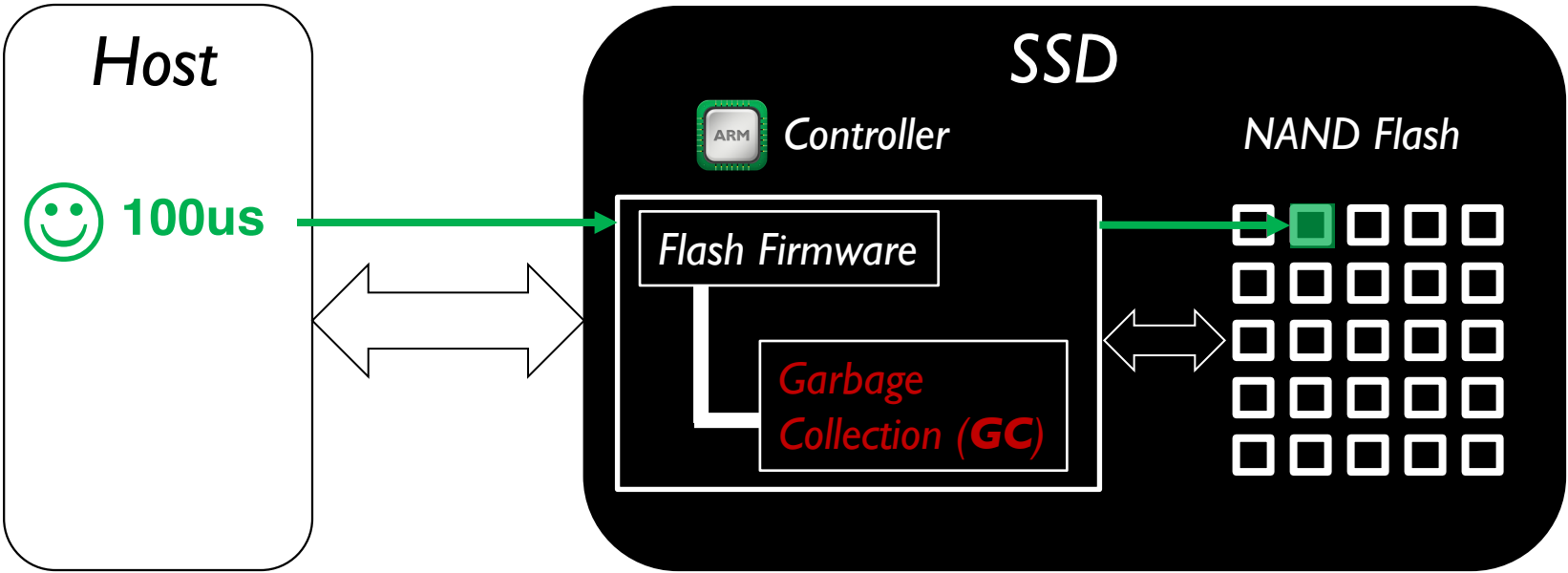


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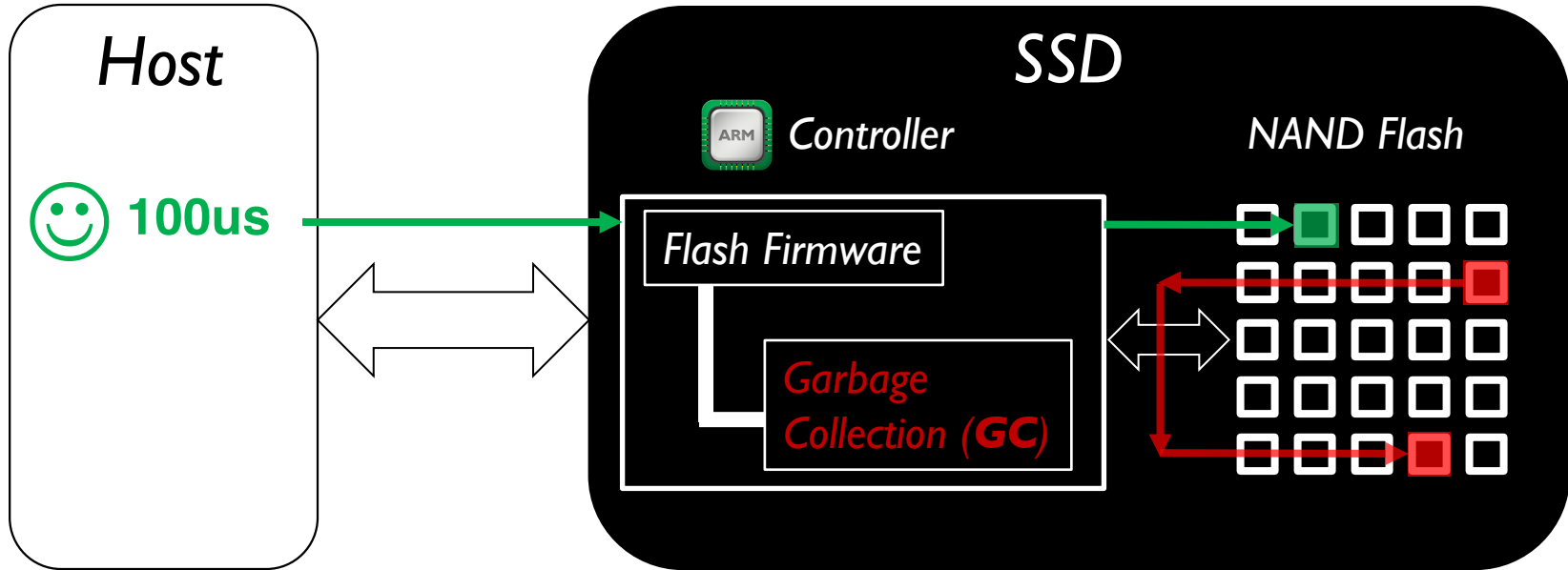




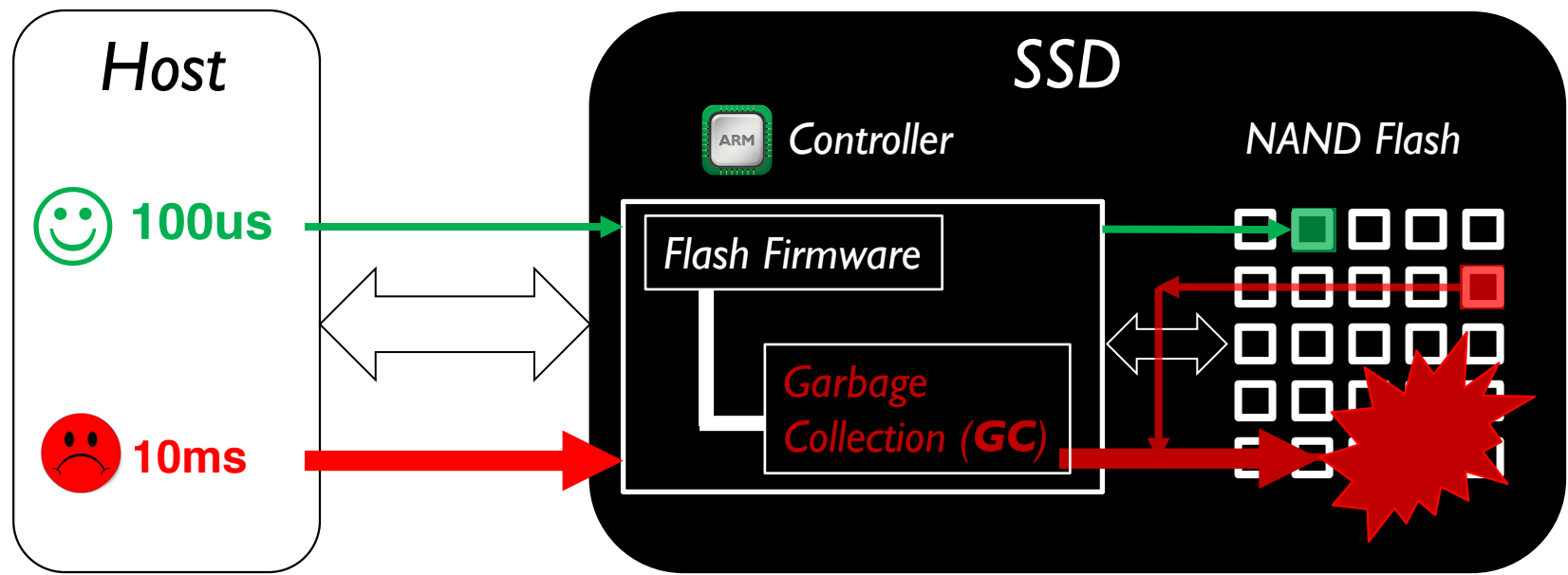
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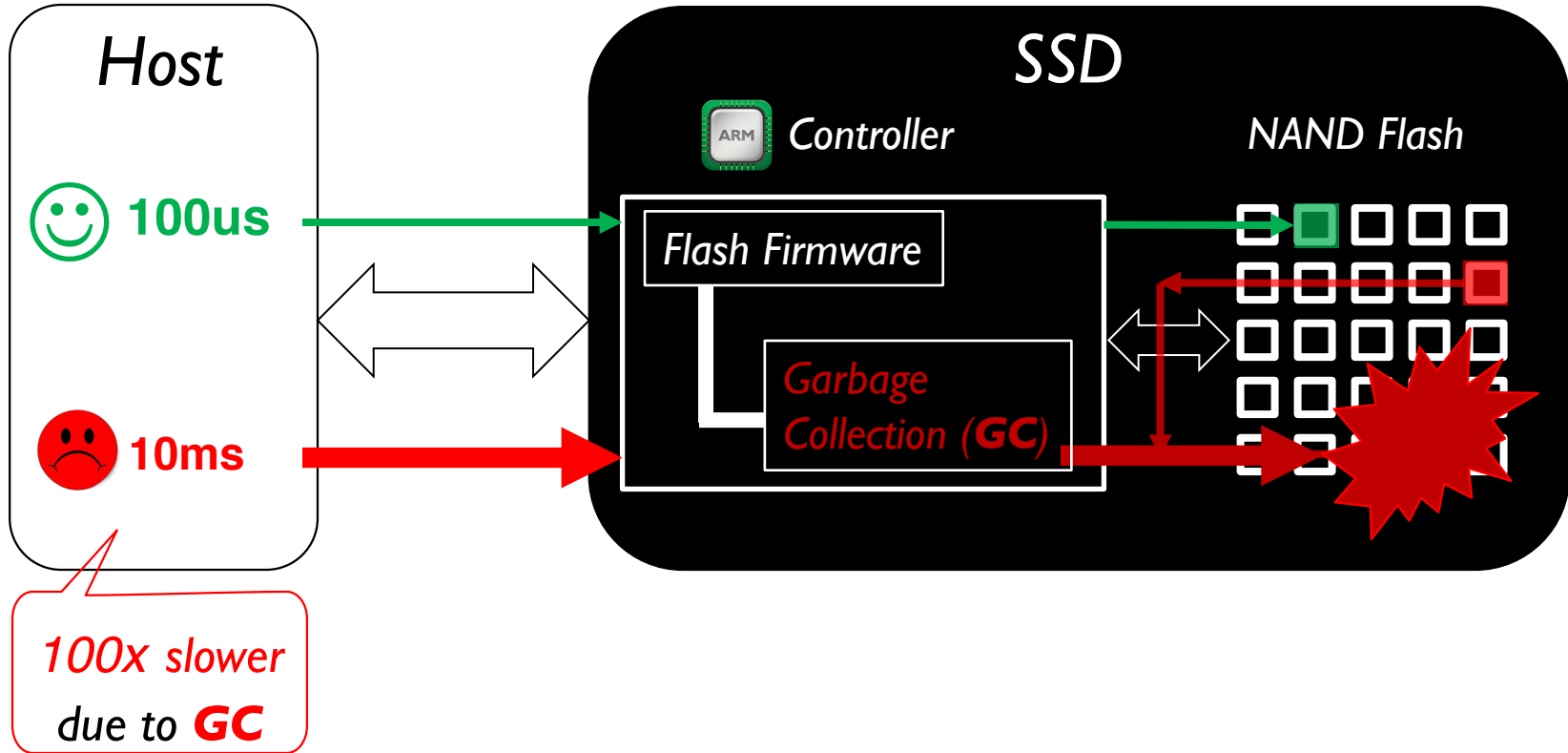
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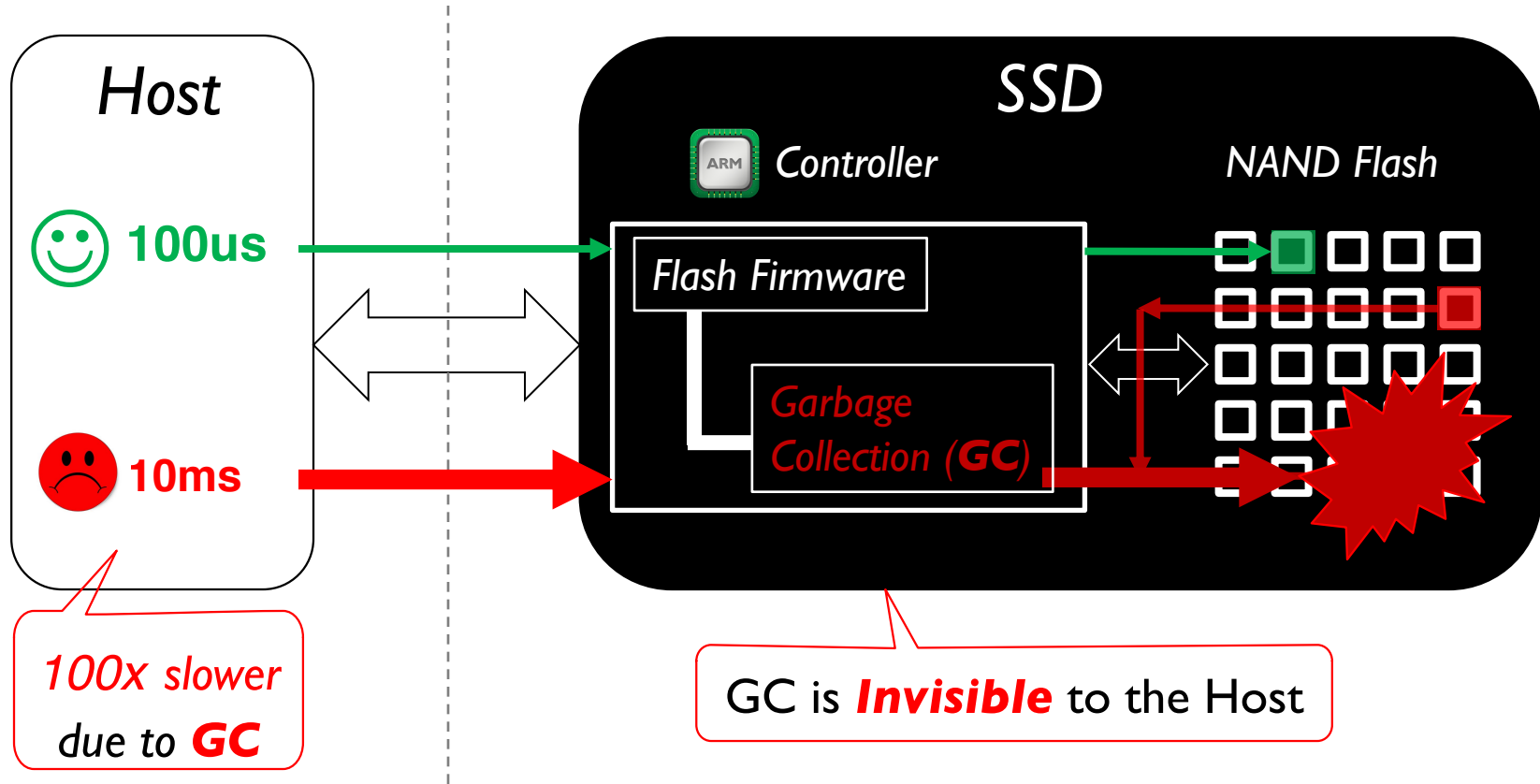
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# *“The Tail Menace”* in Flash Arrays



Host

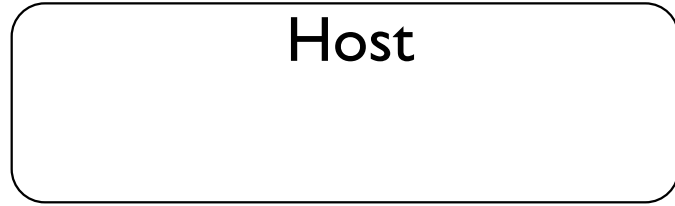
SSD0

SSD1

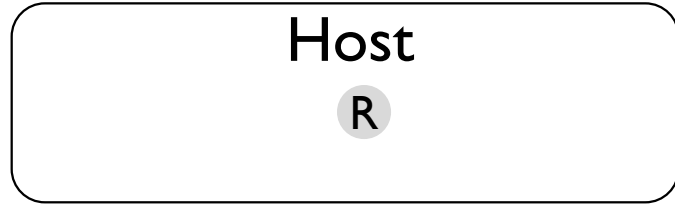
SSD2

SSD3

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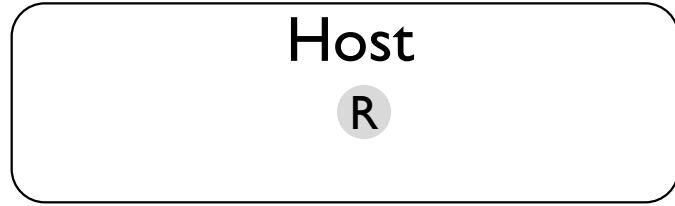


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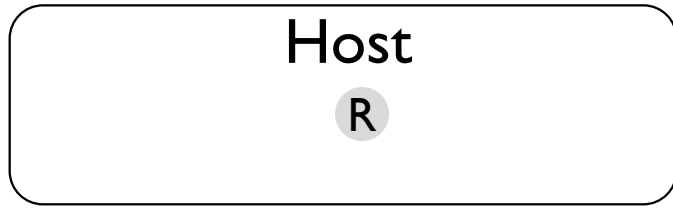




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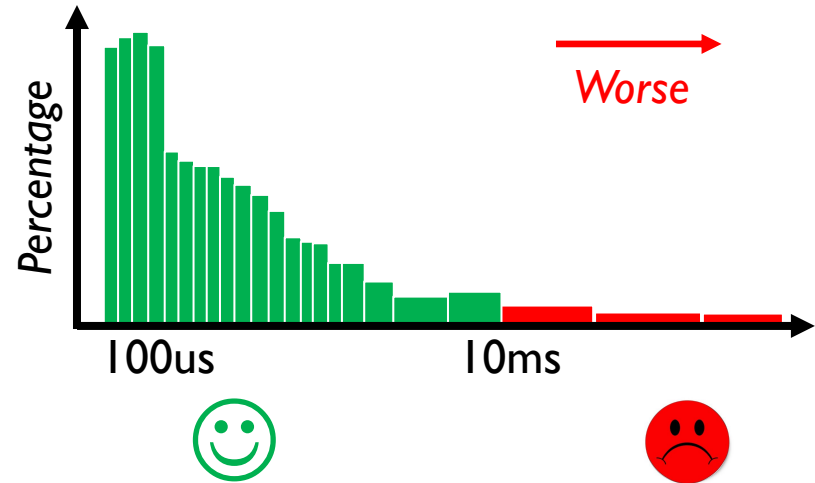
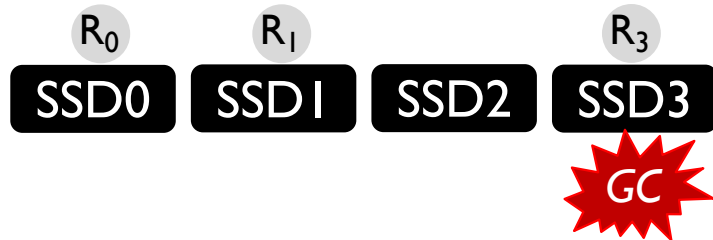
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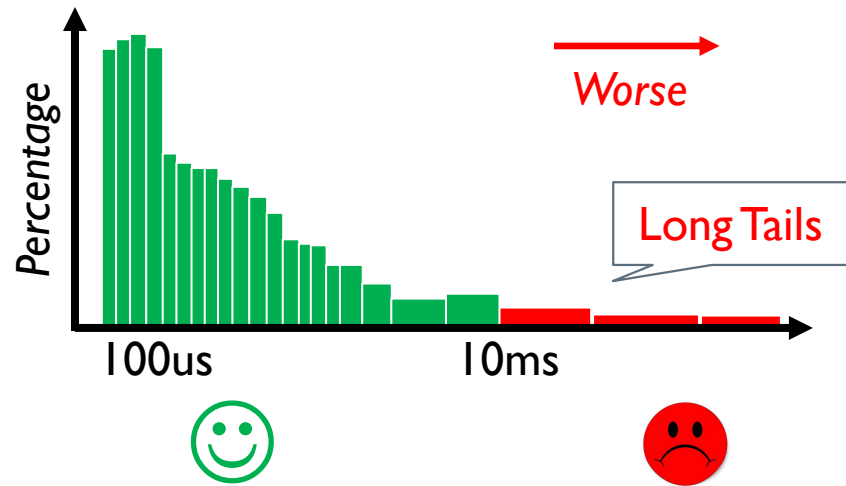
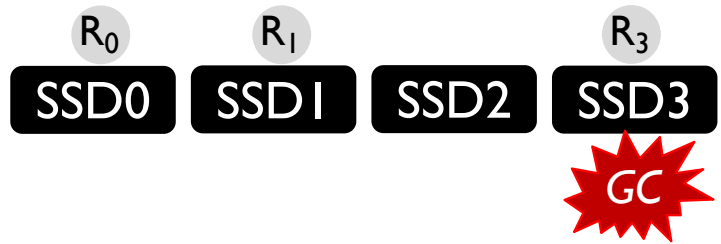
R



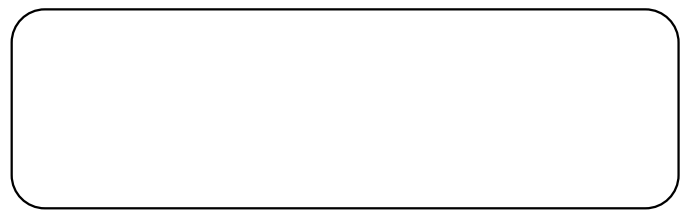
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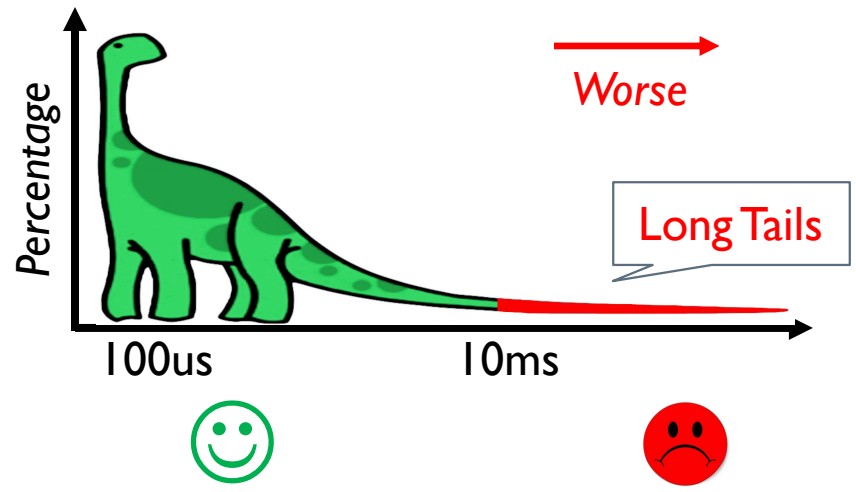
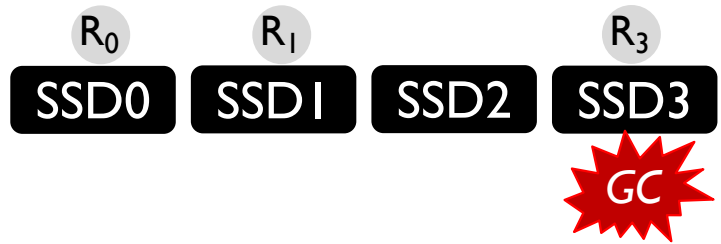
R



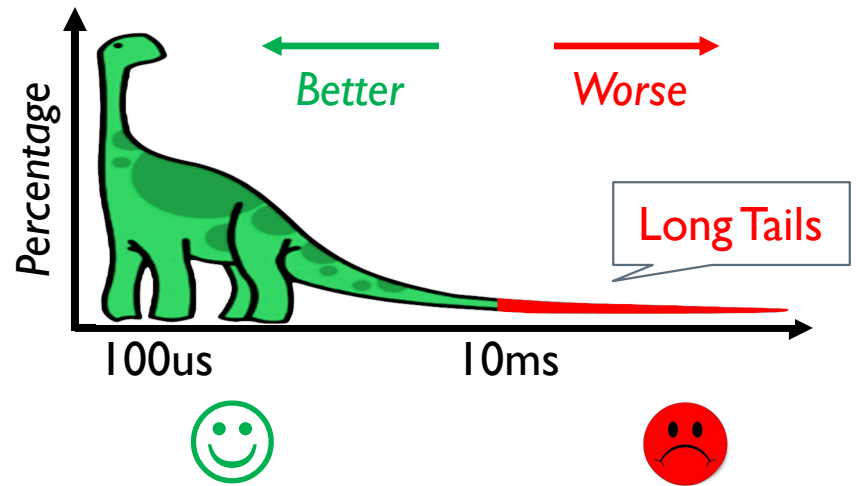
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*A slow SSD makes the entire flash array slow!*



# “*A New Hope*” – NVMe Predictable Latency Mode

NVMe Predictable Latency Mode (***PLM***)

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NVMe Predictable Latency Mode (**PLM**)

A major leap

- + Predictable/Busy *Time Window (TW)*
- + Device status *query & toggling*

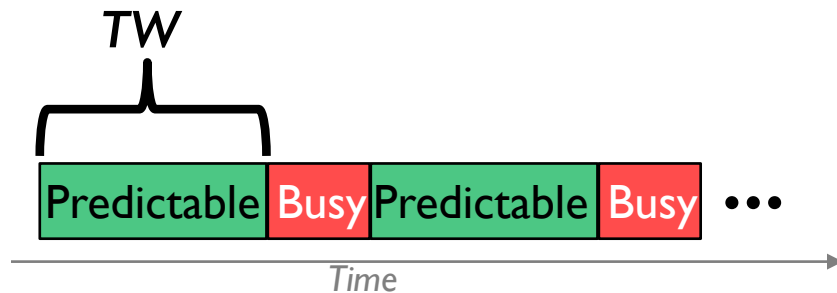


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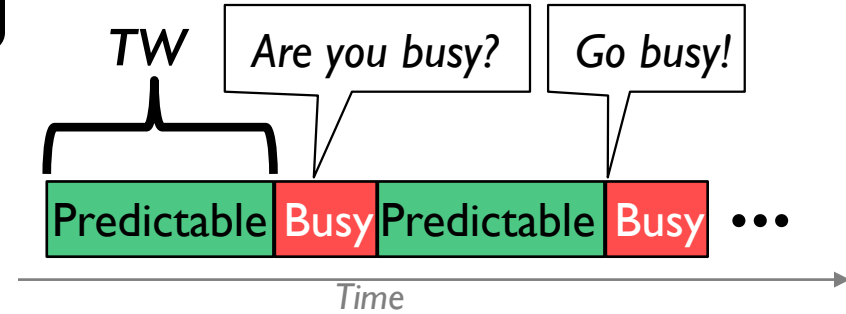


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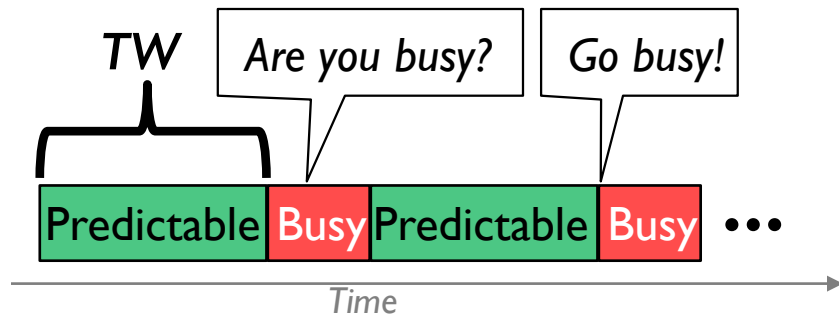
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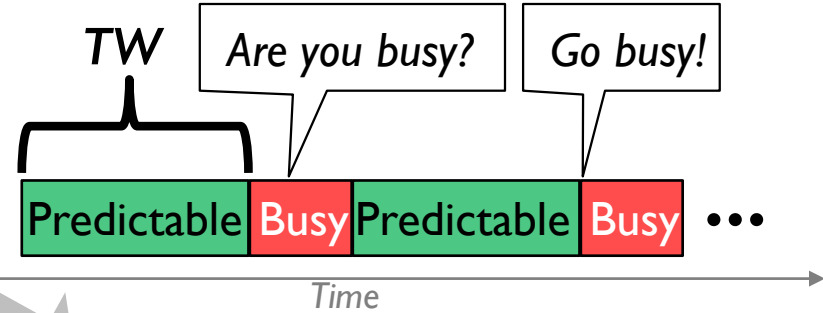
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How to leverage NVMe PLM  
and enhance it  
for predictable latencies?

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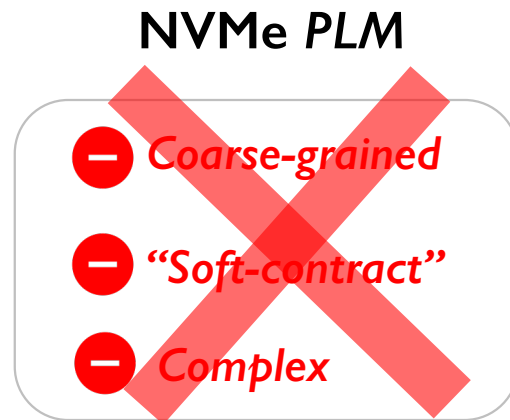
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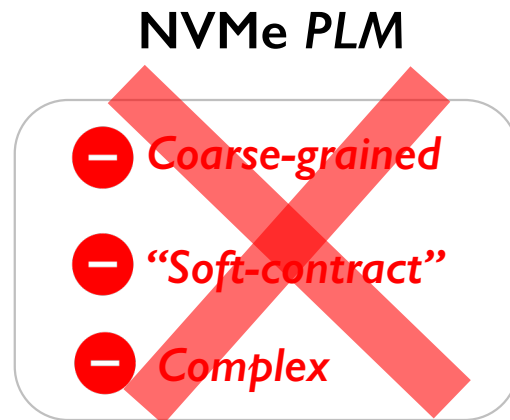
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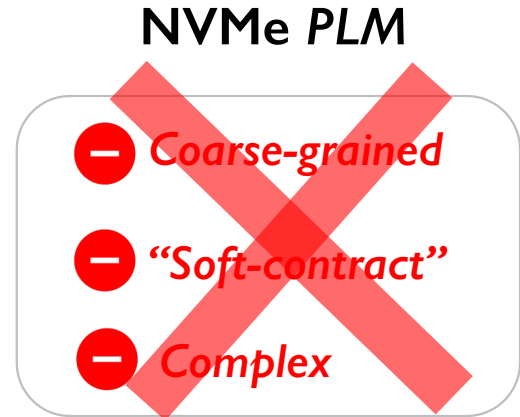
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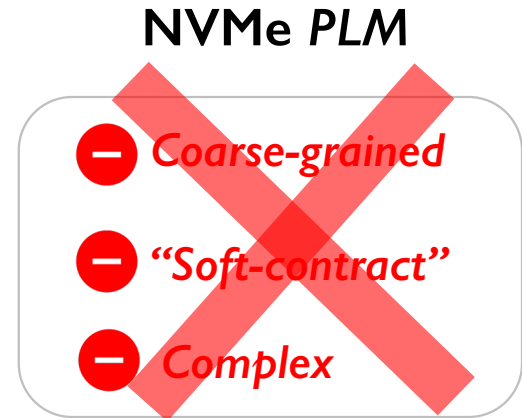
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  - + An end-to-end design exploiting above extensions



- ❑ Background & Motivation
- ❑ IODA Overview
- ❑ IODA Design
  - Predictable latency flagged I/Os
  - Busy remaining time
  - Time window formulation
  - Relaxed TW for better write amplification
- ❑ Evaluation
- ❑ Summary

# Leverage Redundancy for Performance

*An old, effective idea;*

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### Abstract

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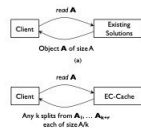


Figure 1: EC-Cache splits individual objects and encodes them using an erasure code to enable read parallelism and late binding during individual reads.

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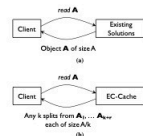


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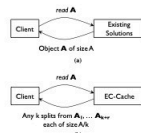


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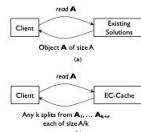


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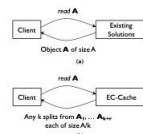


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### Abstract

Data intensive clusters and object stores are increasingly relying on in-memory object caching to meet the I/O performance demands. These systems routinely face the challenges of popularity skew, background load imbalance, and server failures, which result in severe load imbalance across servers and degraded I/O performance. Selective replication is a commonly used technique to tackle these challenges, where the number of cached replicas of an object is proportional to its popularity. In this paper, we explore an alternative approach using erasure coding.

EC-Cache is a load-balanced, low latency cluster cache that uses online erasure coding to overcome the limitations of selective replication. EC-Cache employs erasure coding by: (i) splitting and erasure coding individual objects during writes, and (ii) late binding, wherein obtaining any  $k$  out of  $(k+r)$  splits of an object are sufficient, during reads. As compared to selective replication, EC-Cache improves load balancing by more than  $3\times$  and reduces the median and tail read latencies by more than  $2\times$ , while using the same amount of memory. EC-Cache does so using 10% additional bandwidth and a small increase in the amount of stored metadata. The benefits offered by EC-Cache are further amplified in the presence of background network load imbalance

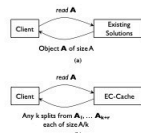


Figure 1: EC-Cache splits individual objects and encodes them using an erasure code to enable read parallelism and late binding during individual reads.

ping [12, 16, 52] and compression [15, 27, 53, 79] are some of the popular approaches employed to increase the effective memory capacity. (iii) Ensuring good I/O performance for the cached data in the presence of skewed popularity, background load imbalance, and failures.

Typically, the popularity of objects in cluster caches are heavily skewed [30, 47], and this creates signif-

# Leverage Redundancy for Performance

An old, effective idea;

Yet, challenging for PLM

## When to issue the parity reads?

(1) *Wait* for timeout

– Best threshold? *Tricky*

(2) *Always Proactive* (always send full-stripe)

– Increased load  $\rightarrow$  *Inefficient*

Semantic gap between the Host and SSD to communicate the “busyness”

Tiny-Tail Flash: Near-Perfect Elimination of Garbage Collection Tail Latencies in NAND SSDs

Trimming the Tail for Deterministic Read Performance in SSDs

Latency Reduction and Load Balancing in Coded Storage Systems

RAIL: Predictable, Low Tail Latency for NVMe Flash

MittOS: Supporting Millisecond Tail Tolerance with Fast Rejecting SLQ-Aware OS Interface

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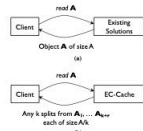


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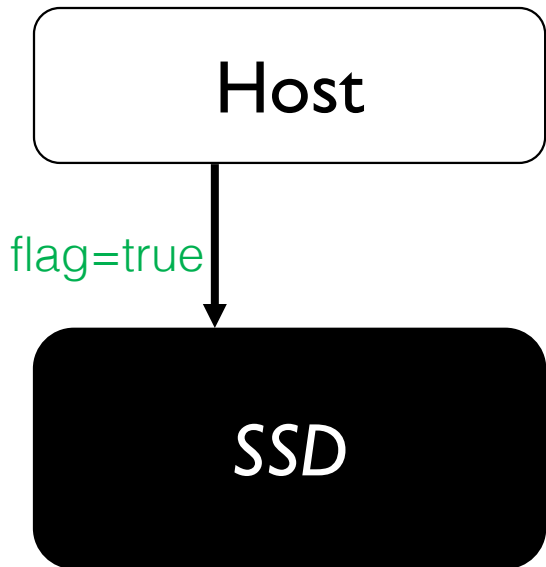
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Host

SSD

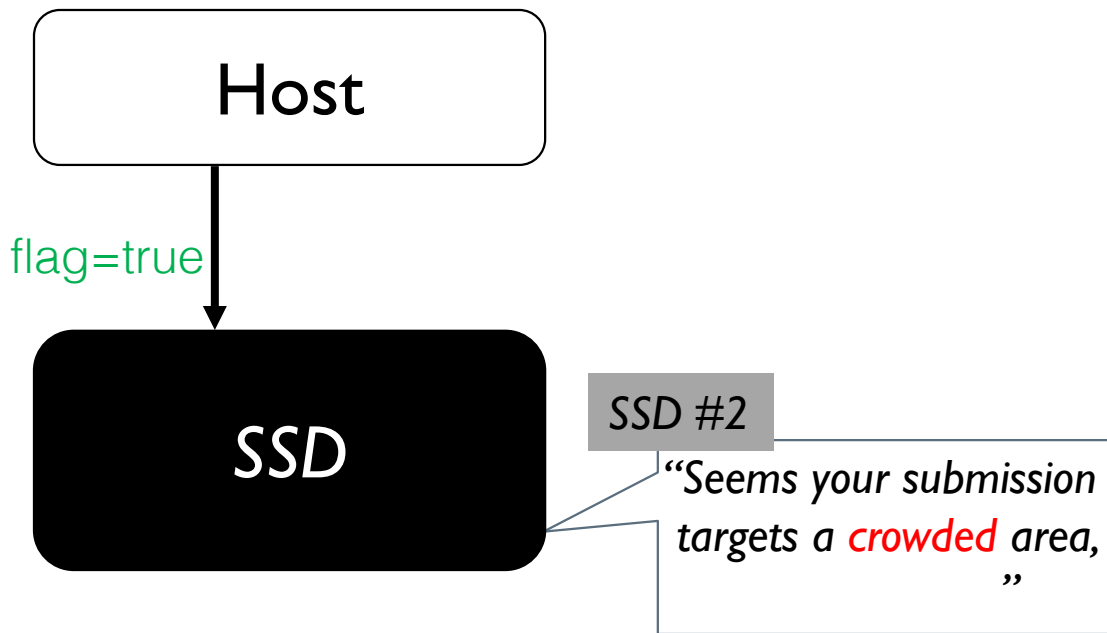
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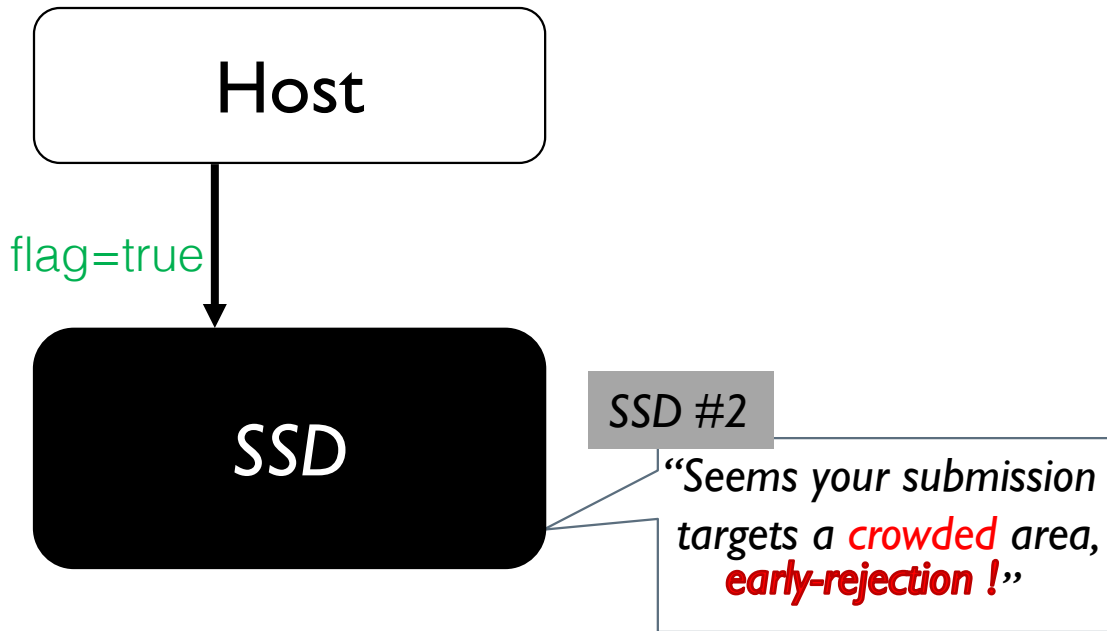
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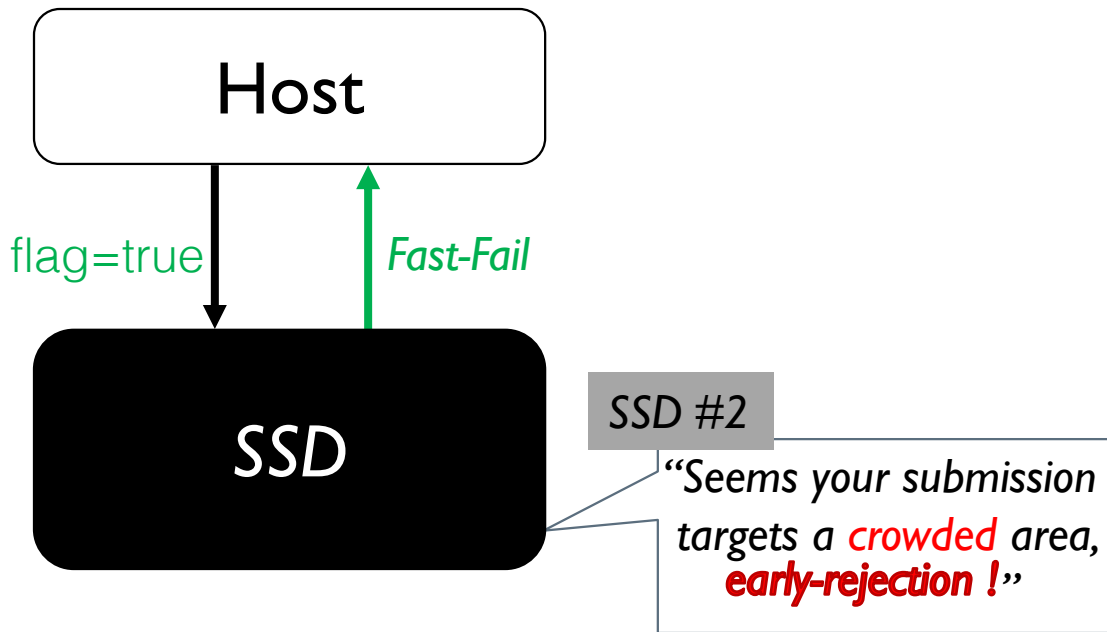
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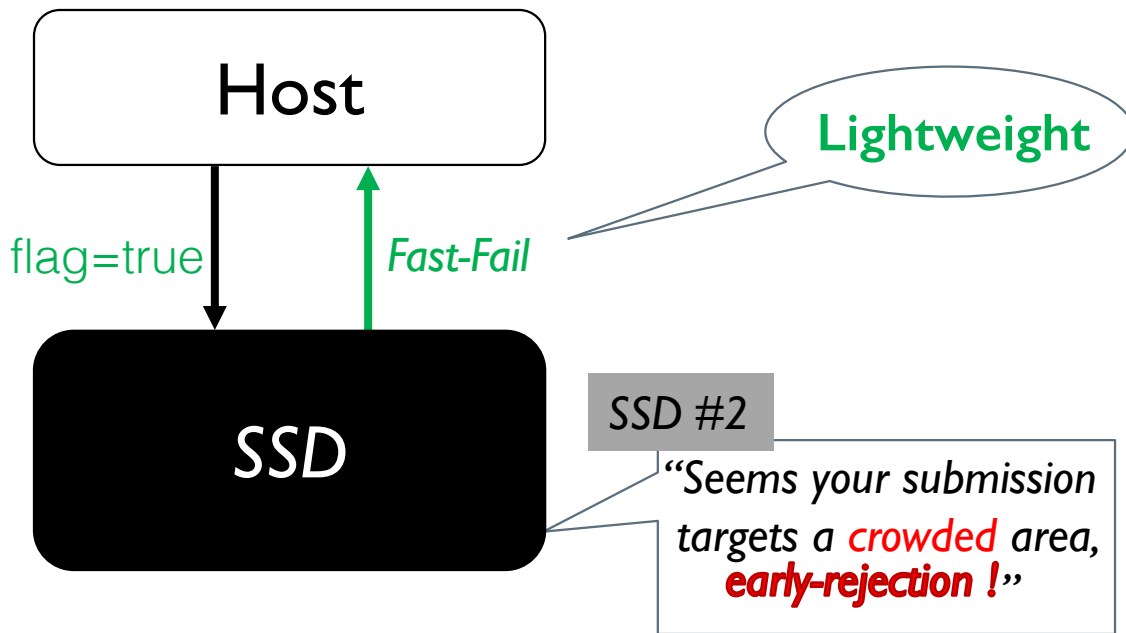
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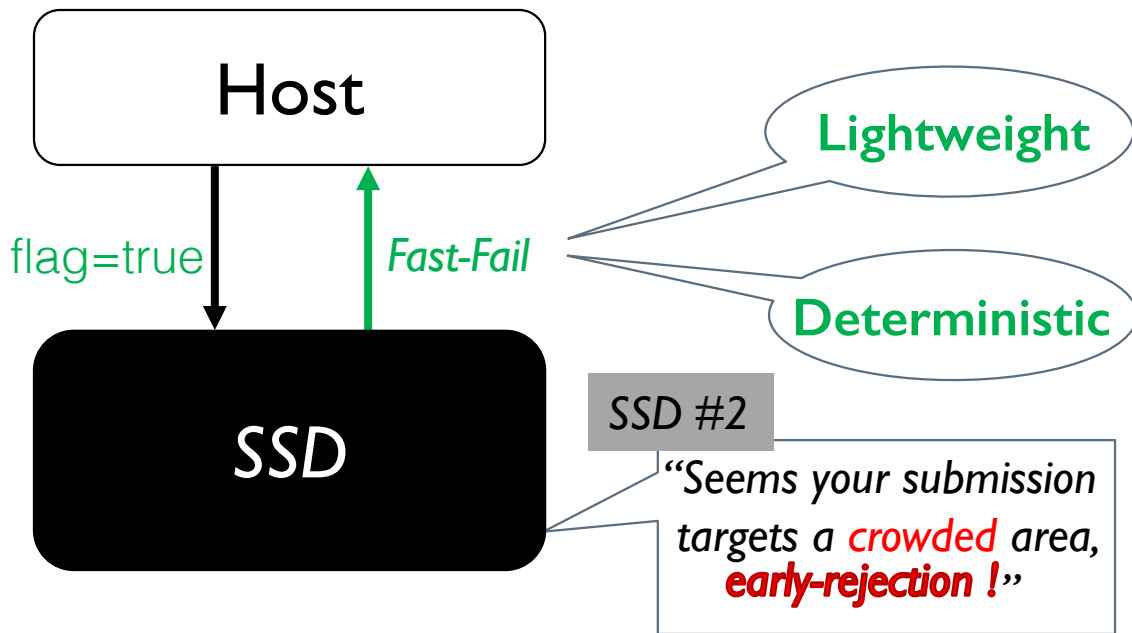
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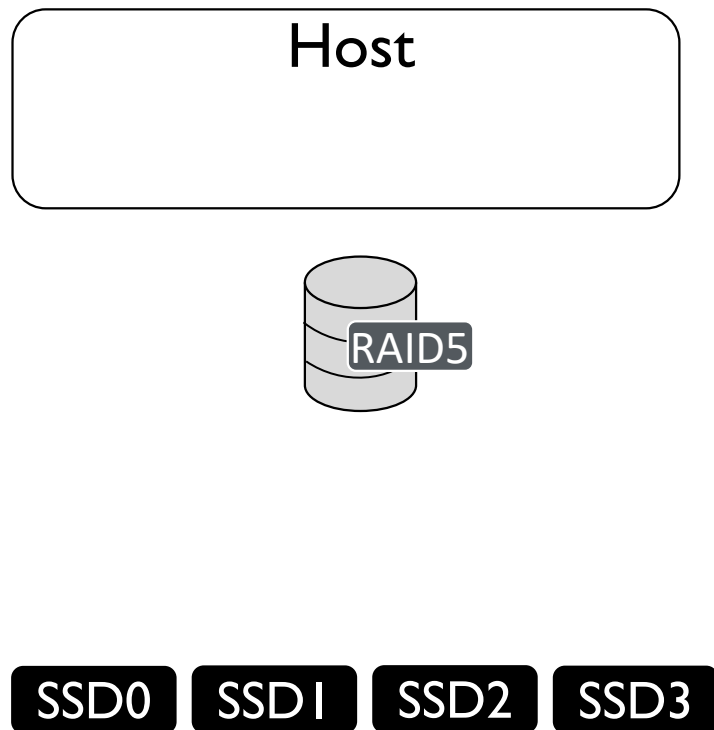
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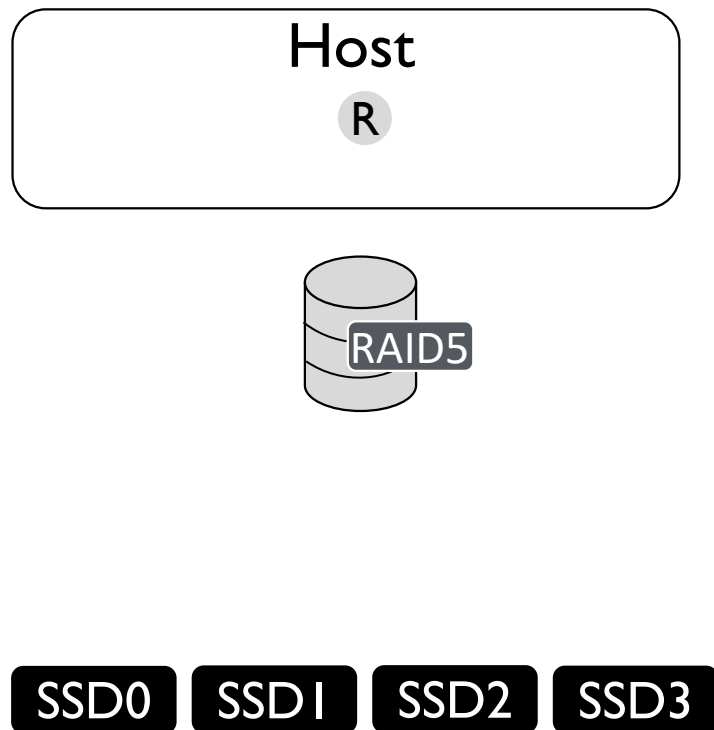


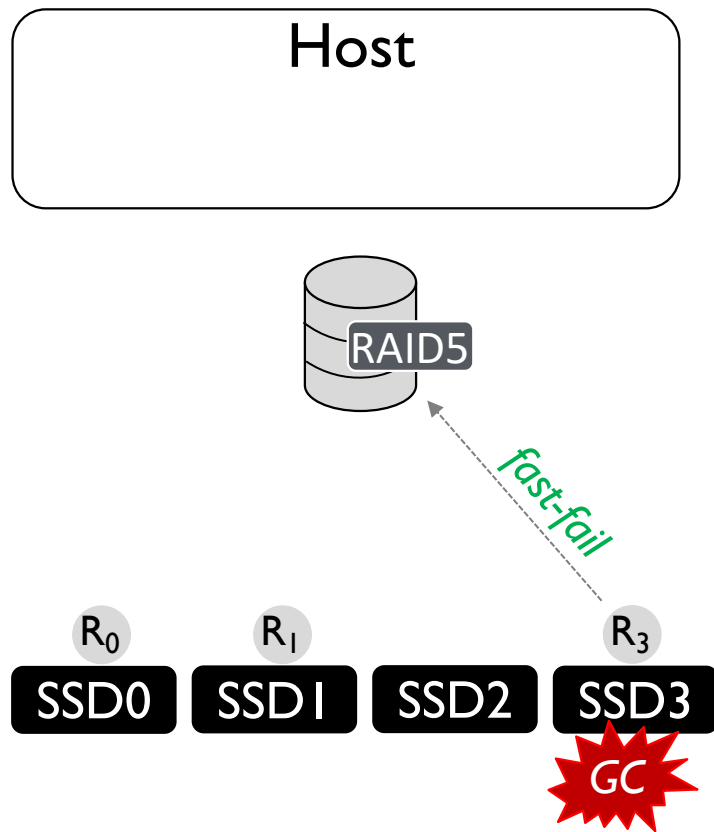
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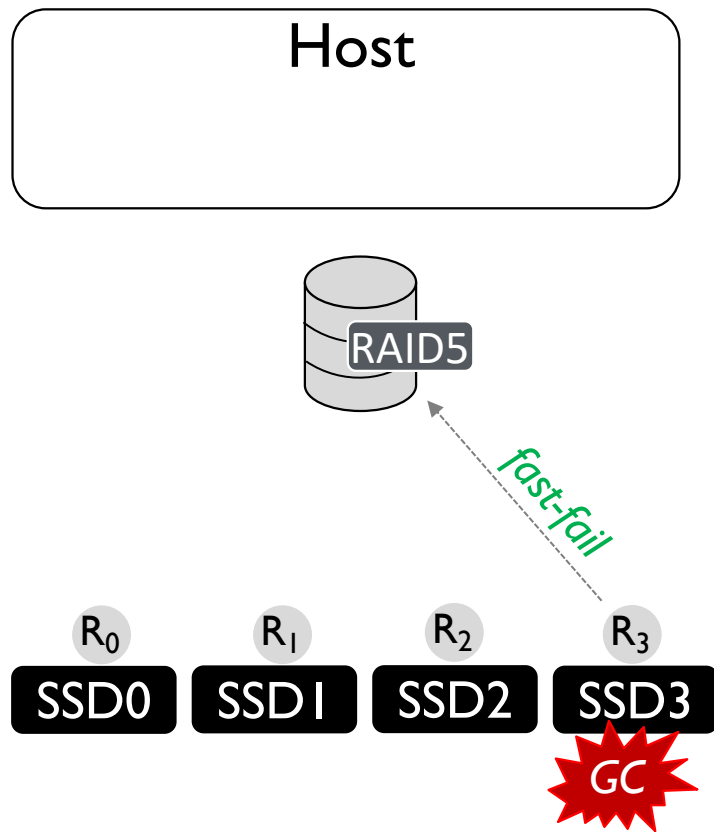
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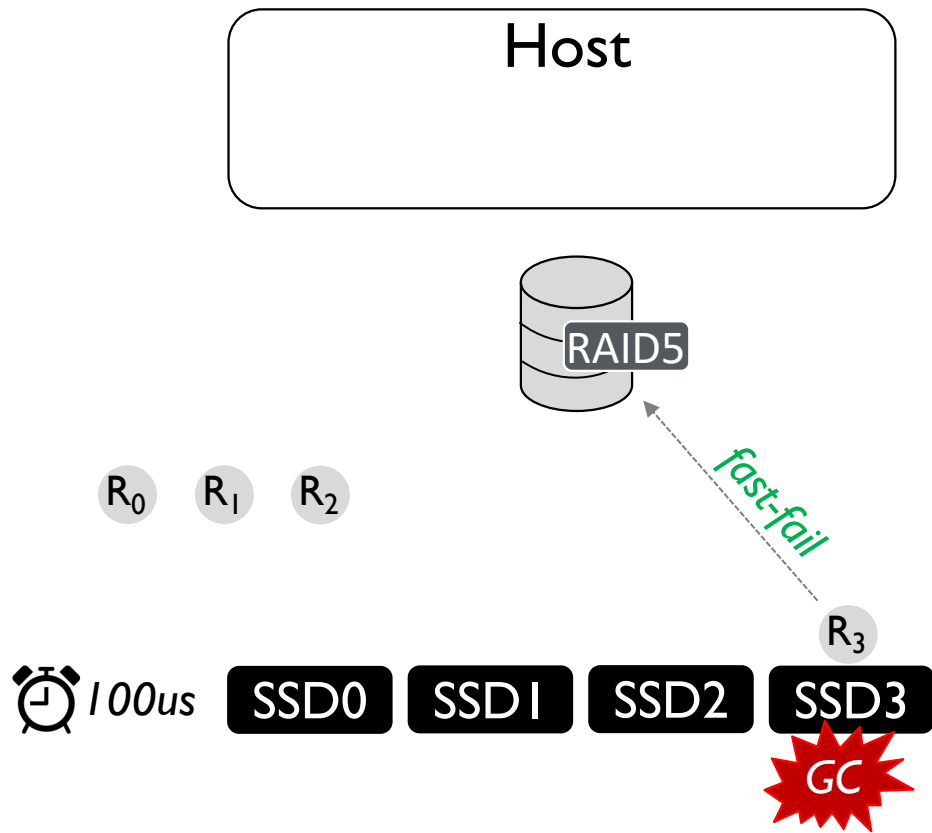




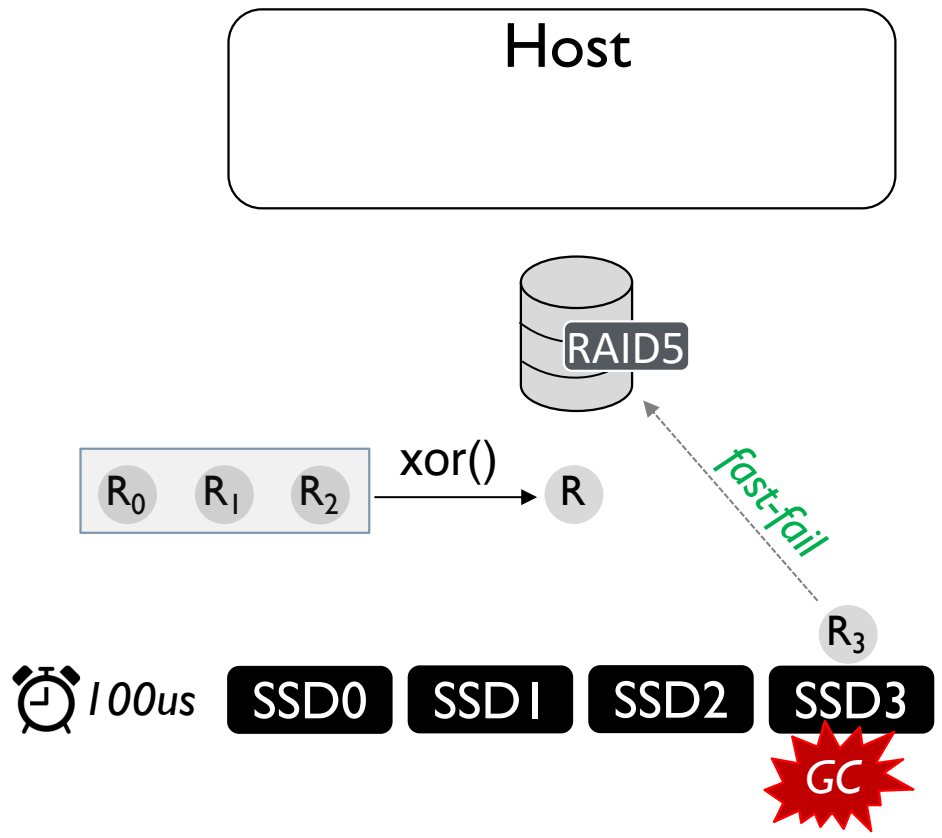


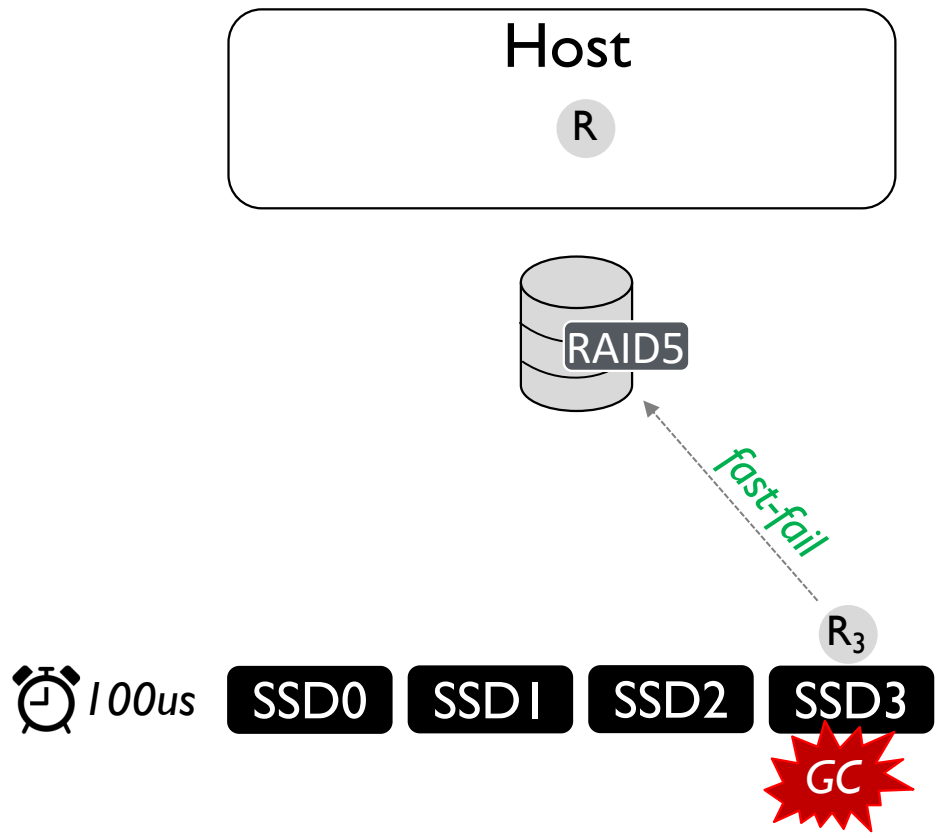


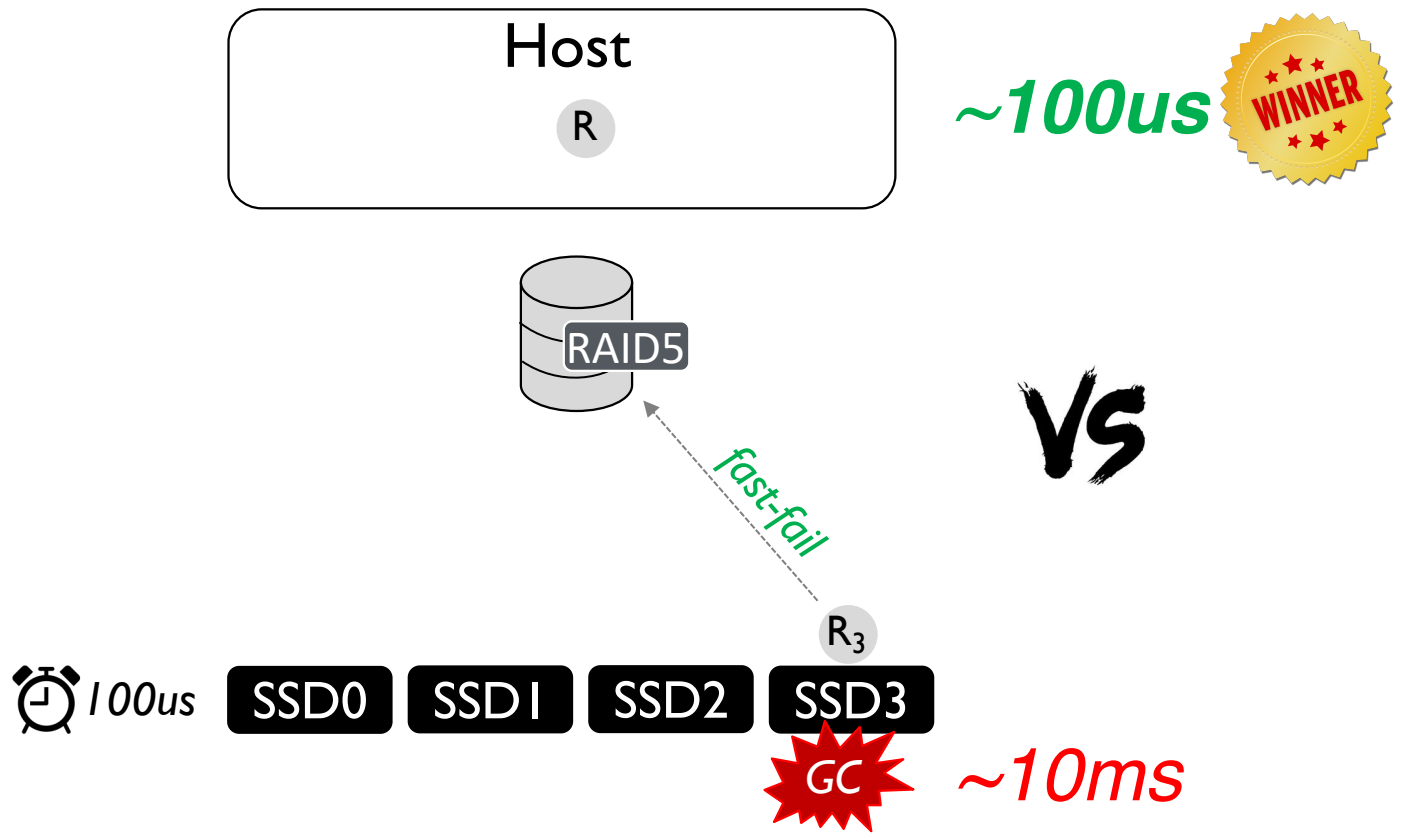




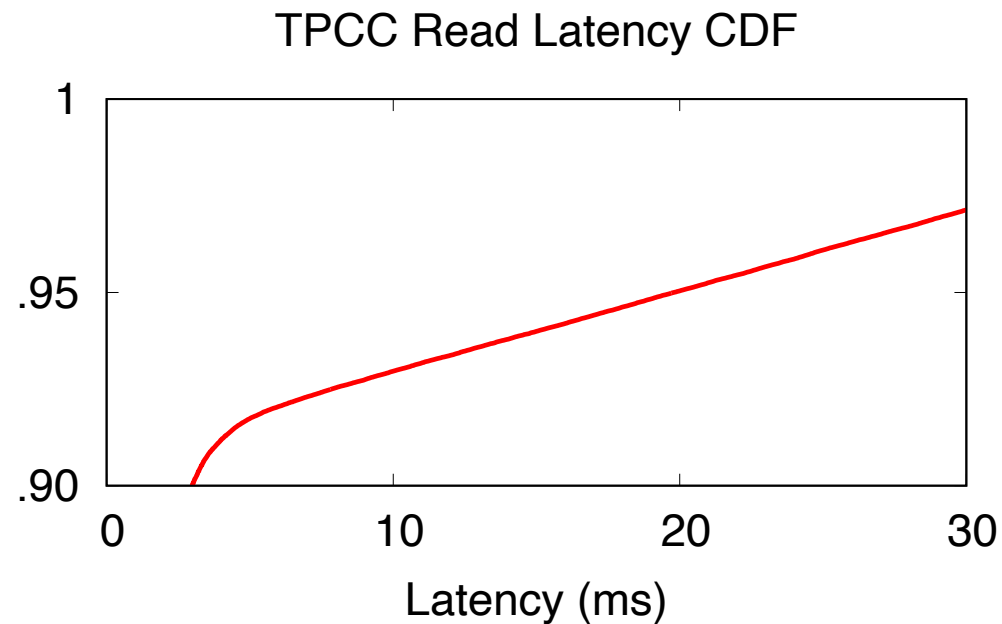




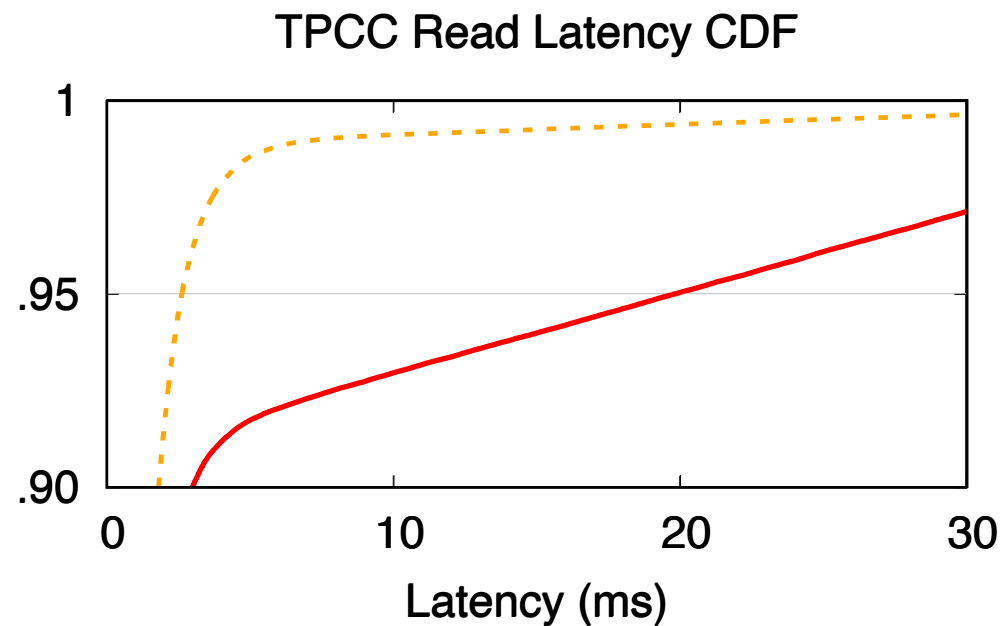




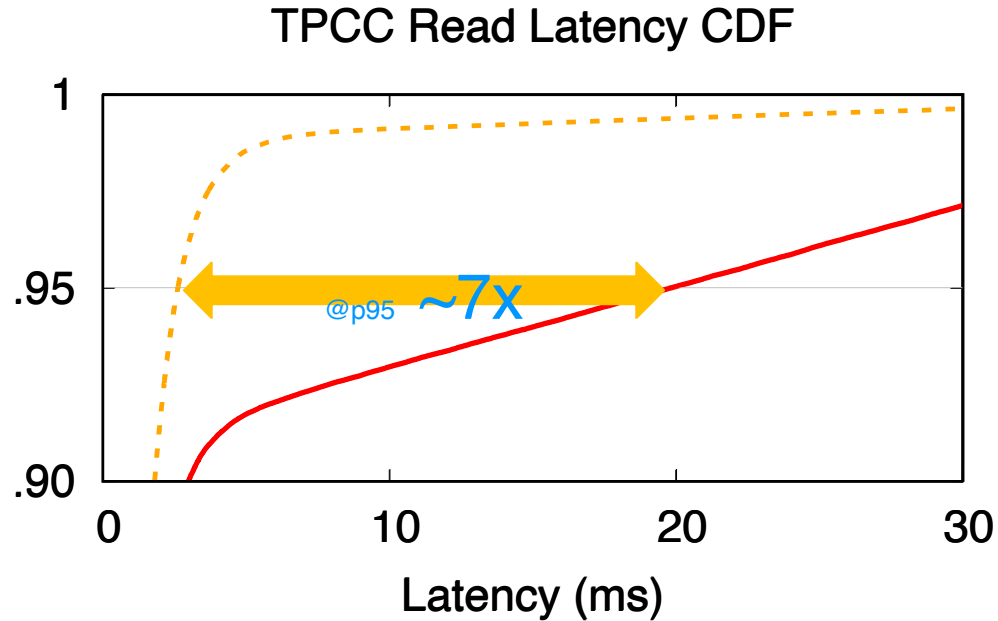
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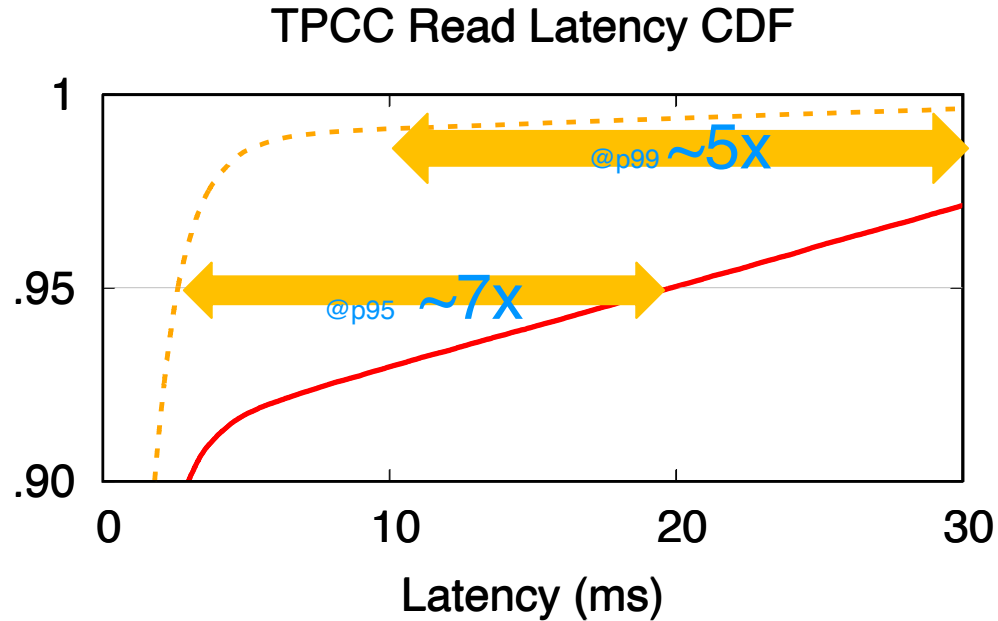
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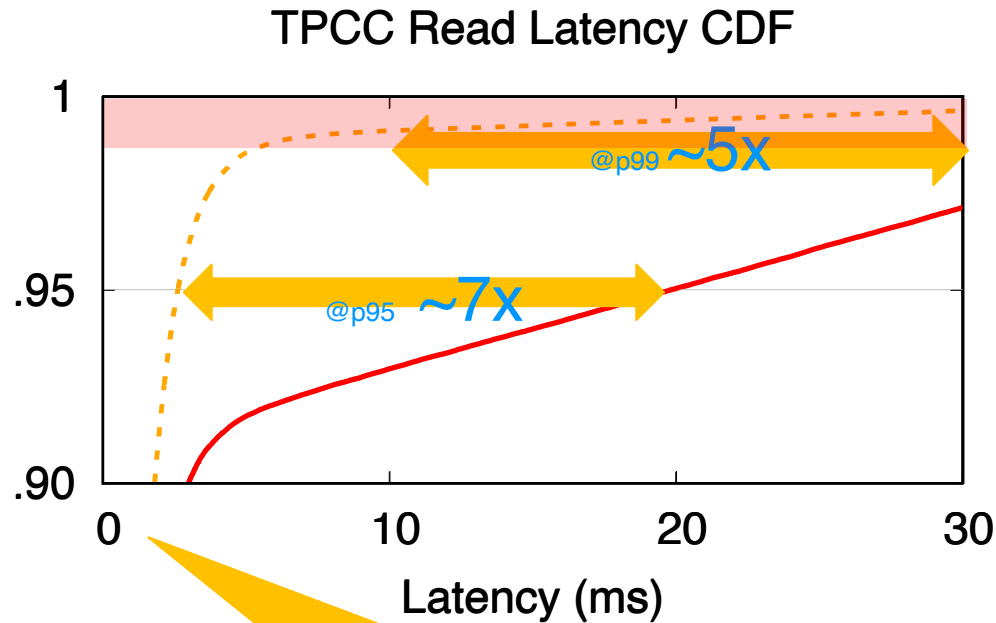
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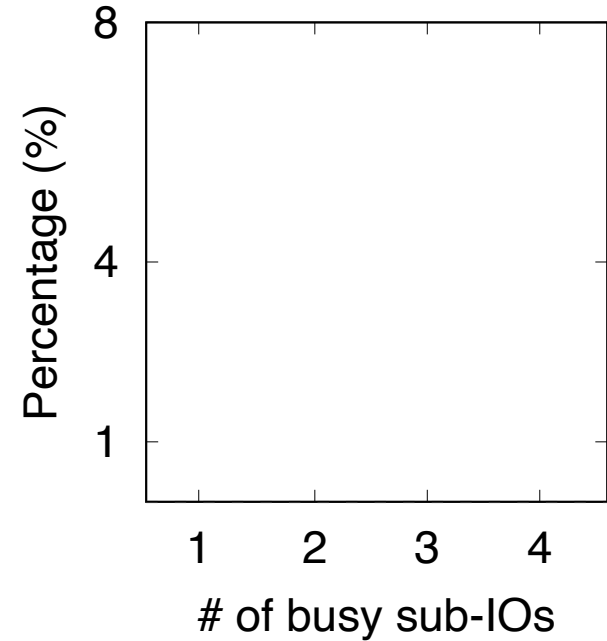
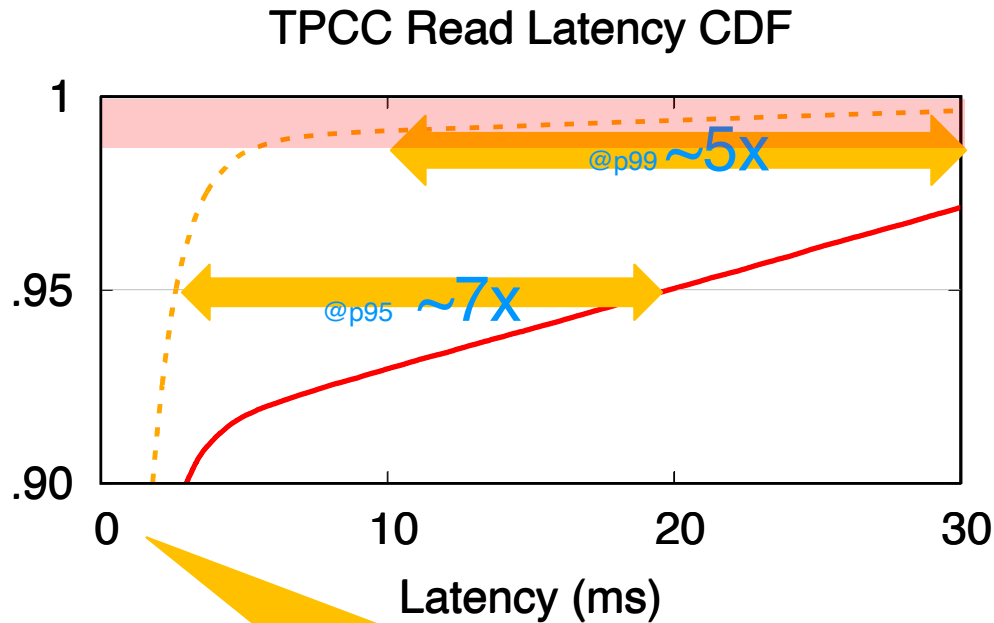
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*Cut tails up to ~99<sup>th</sup> percentile*

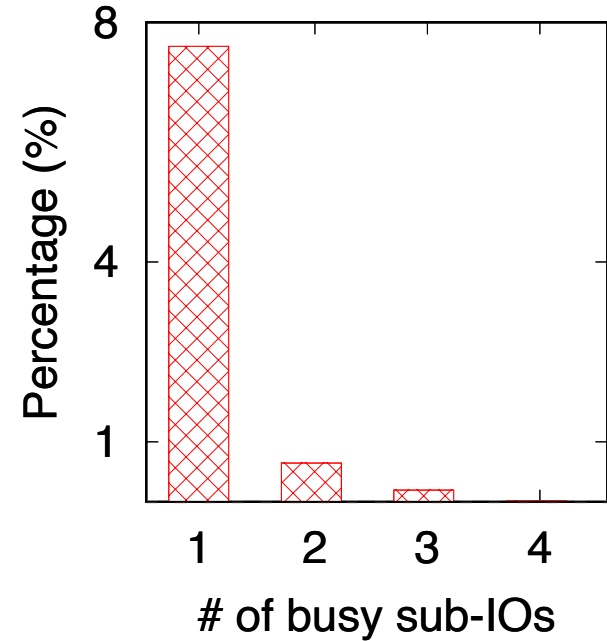
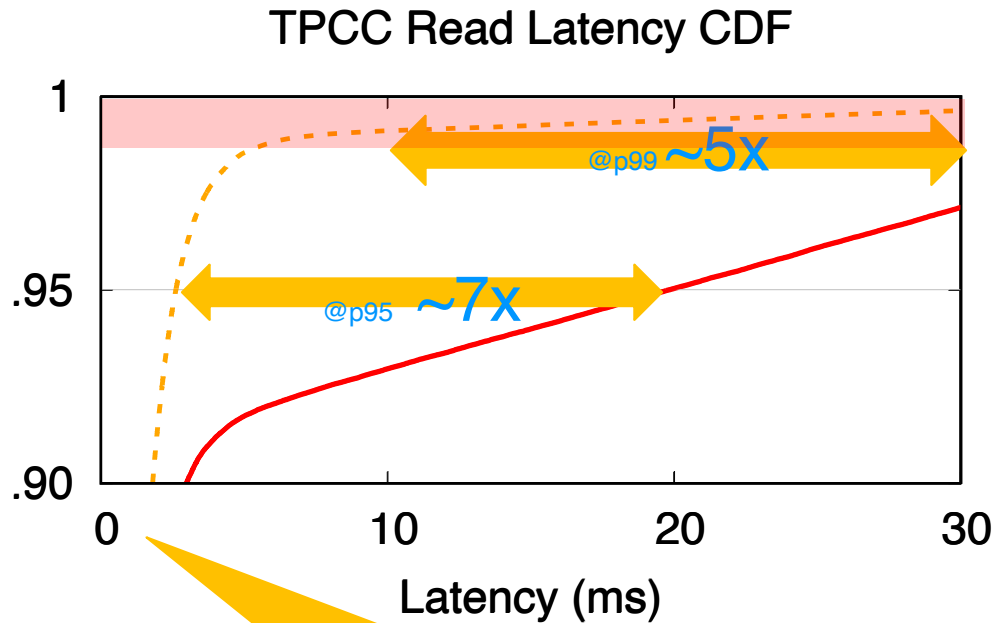


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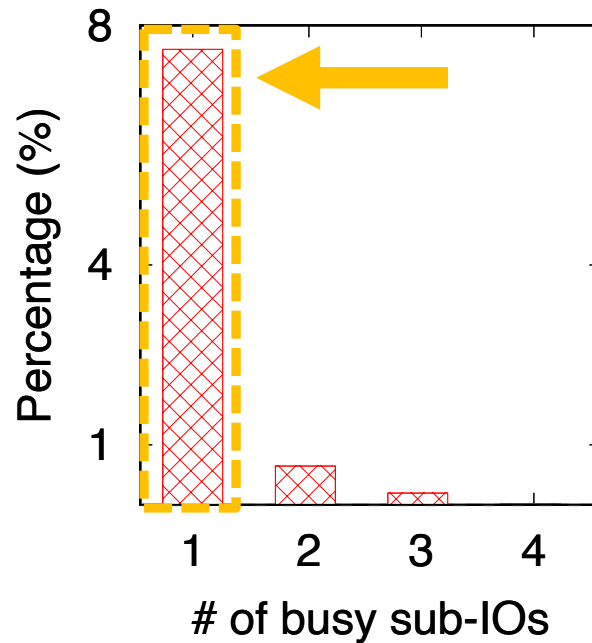
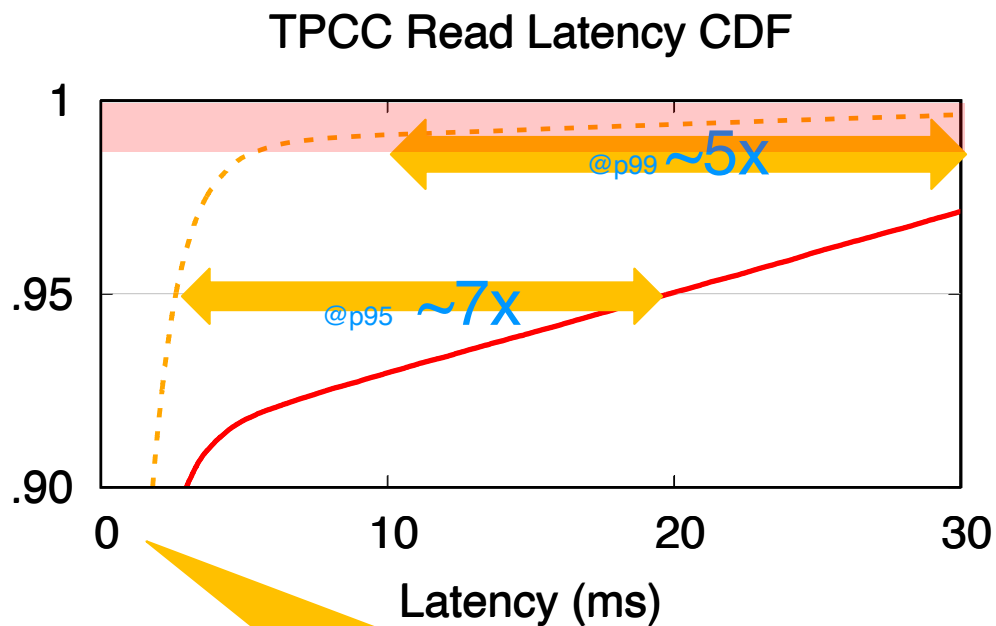
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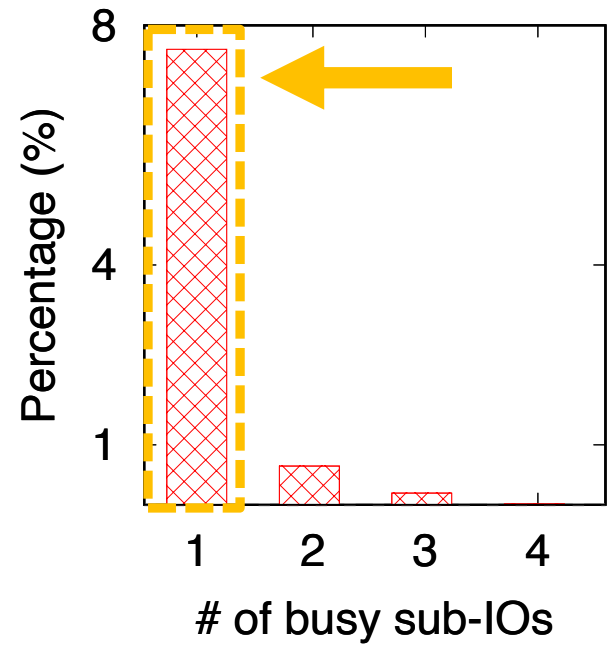
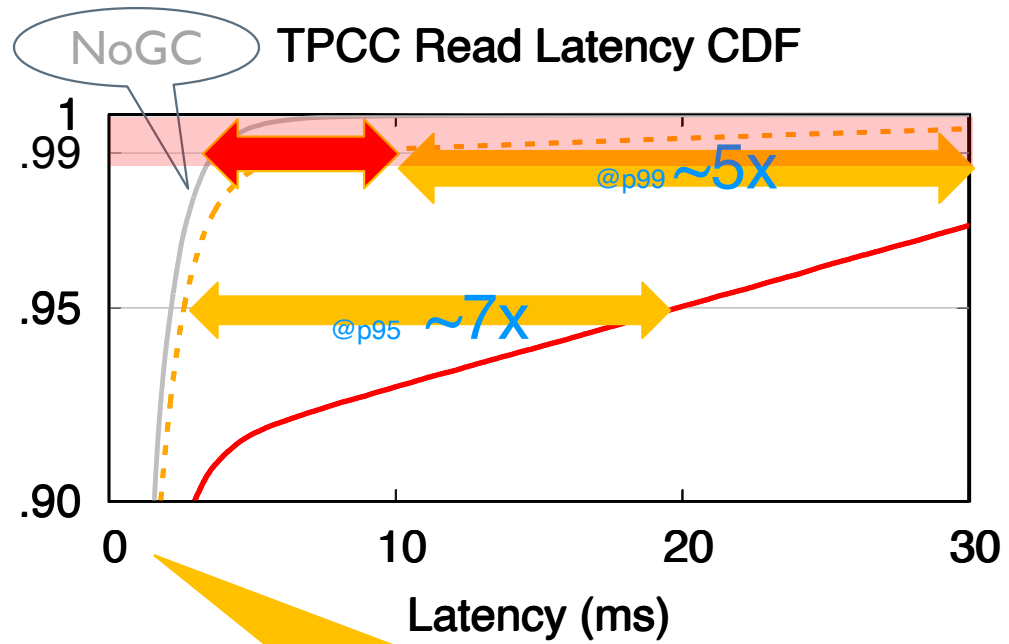
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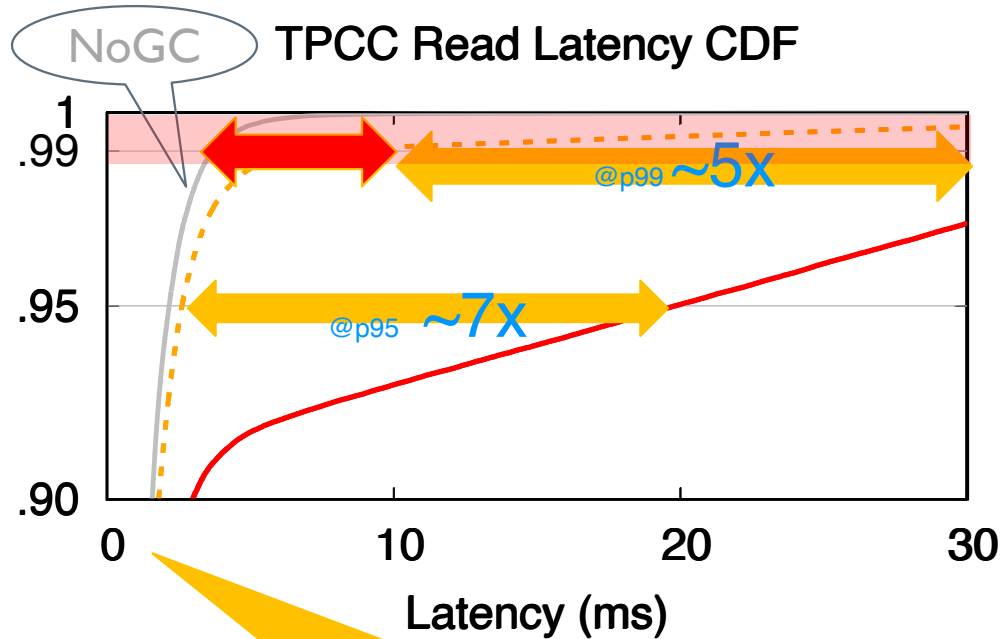
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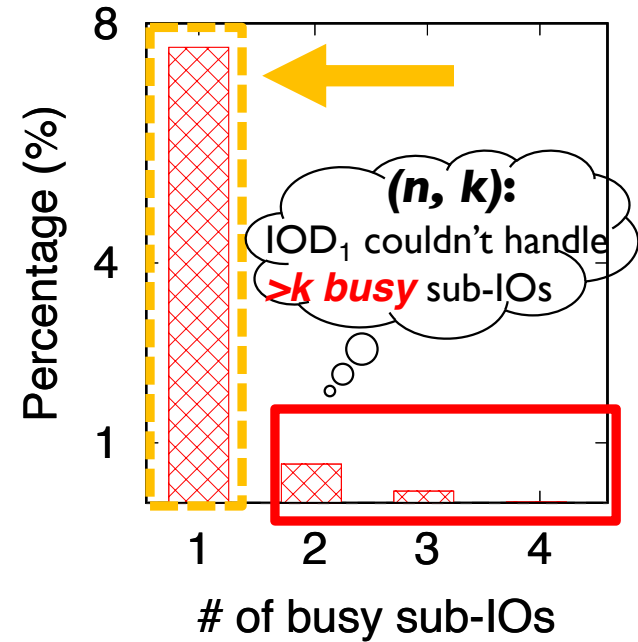


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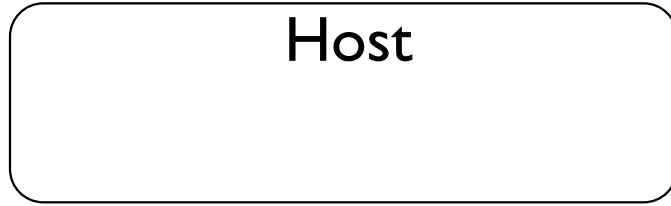
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# A Case Against Proactive Reconstruction

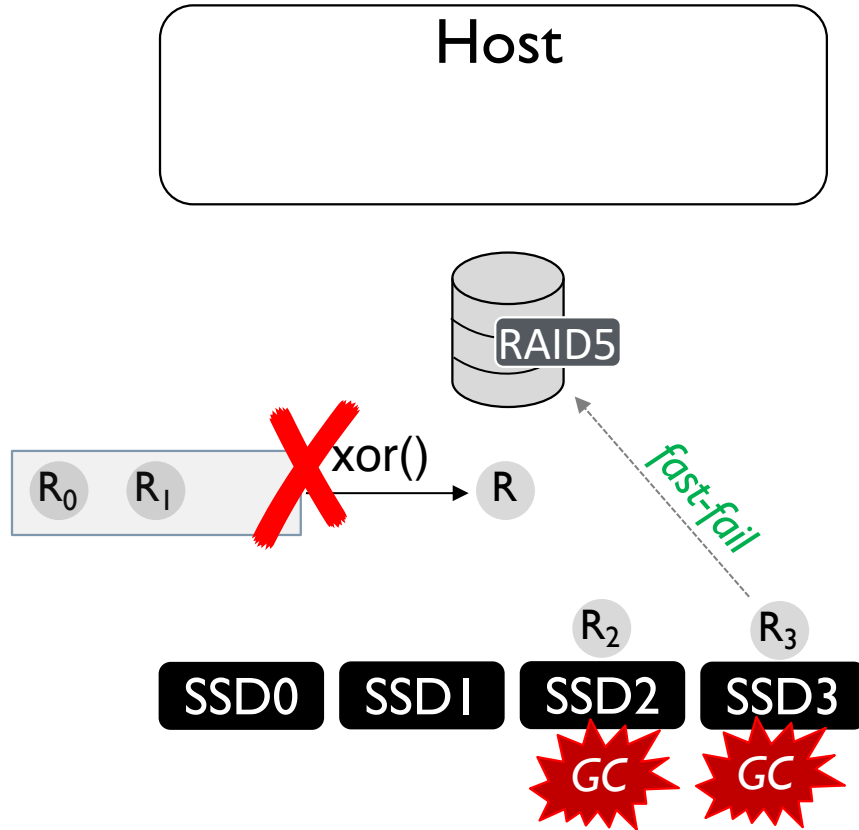




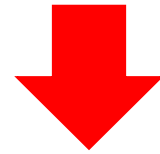




# A Case Against Proactive Reconstruction



**Semantic Gap:** the host doesn't know how long SSD "busyness" will last



End up waiting for the busiest SSD

# Busy Remaining Time (BRT) Exposure



“*Fail-if-Slow*”: the SSD should *fast-fail* an I/O if it contends with GC



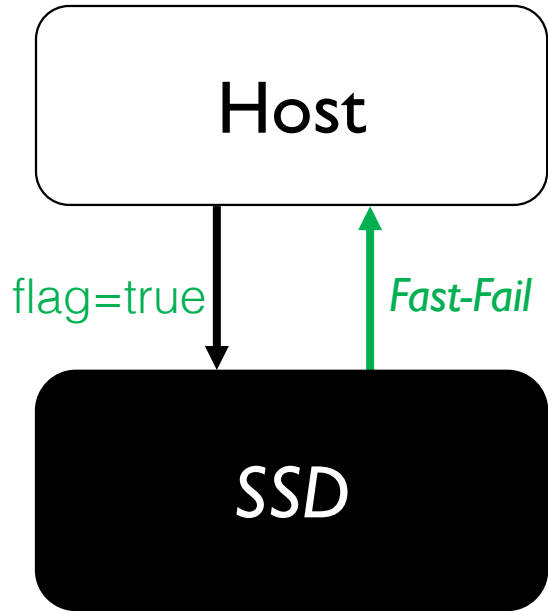
Piggybacking **BRT** to reconstruct data from less busy SSDs

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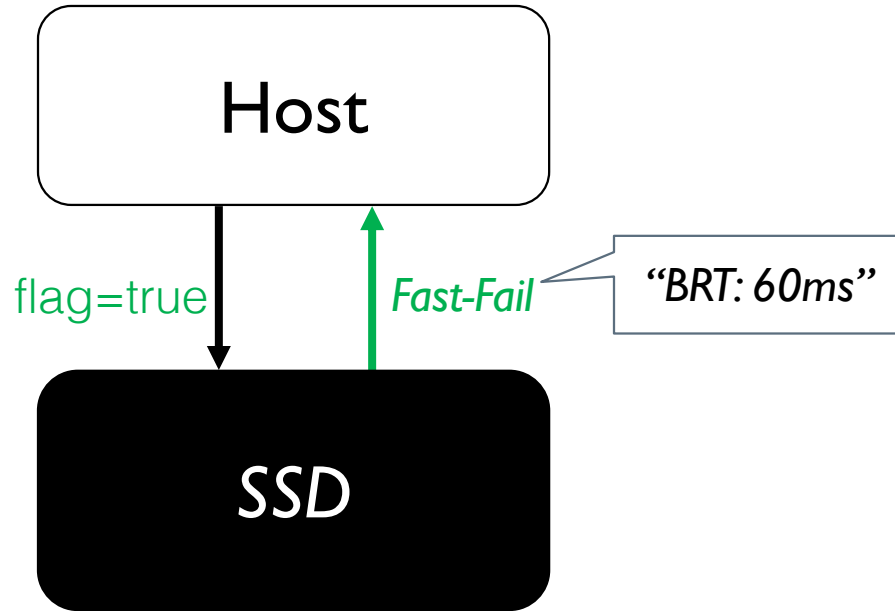
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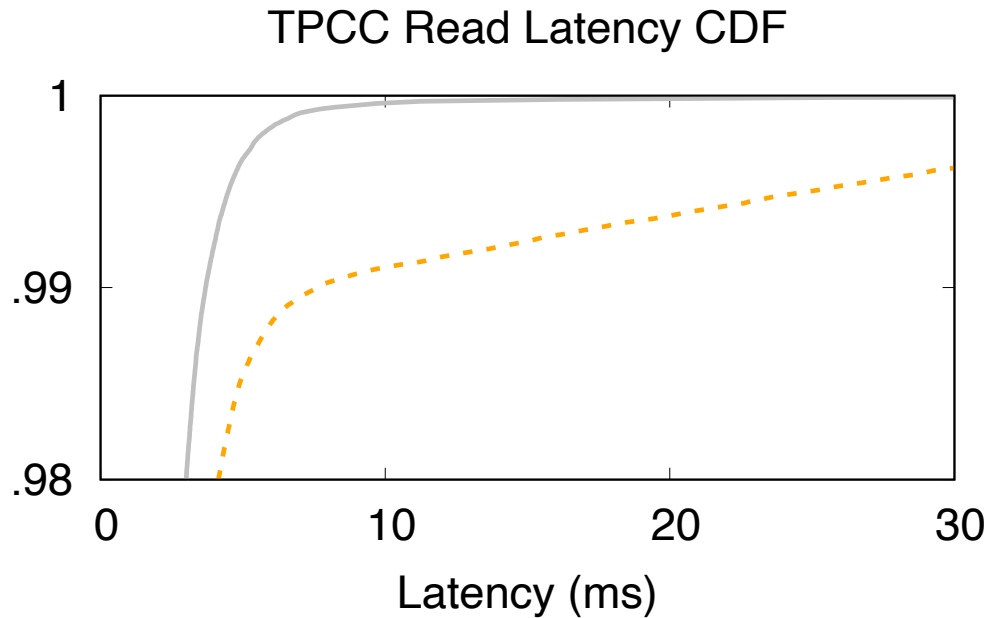


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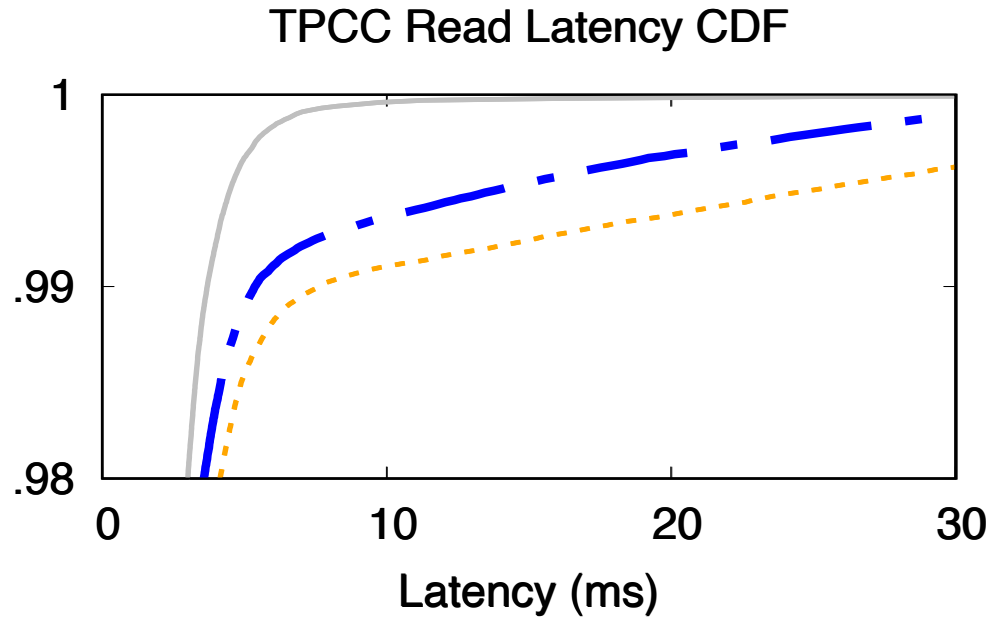


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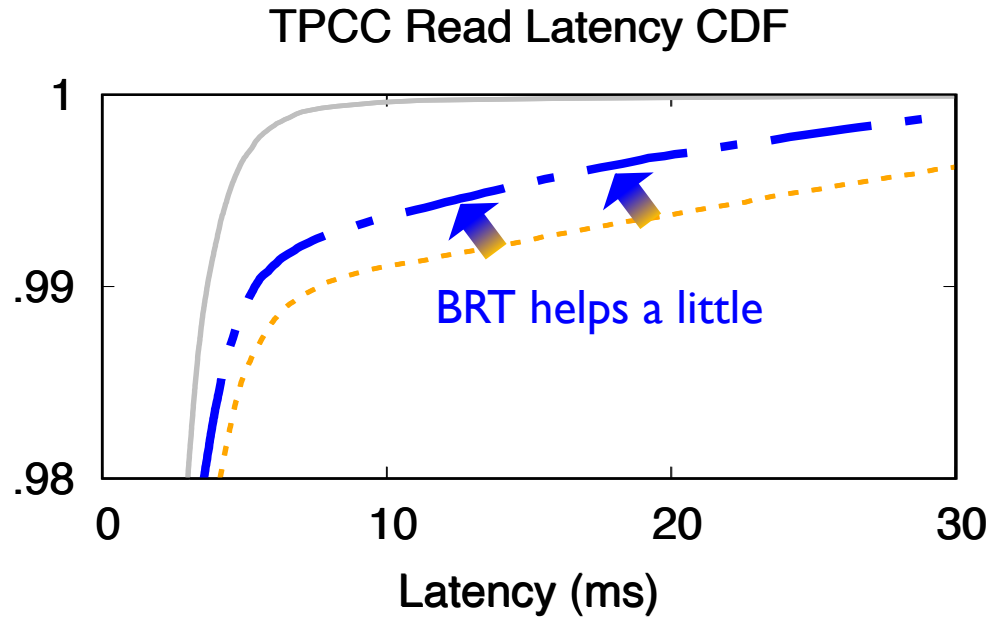
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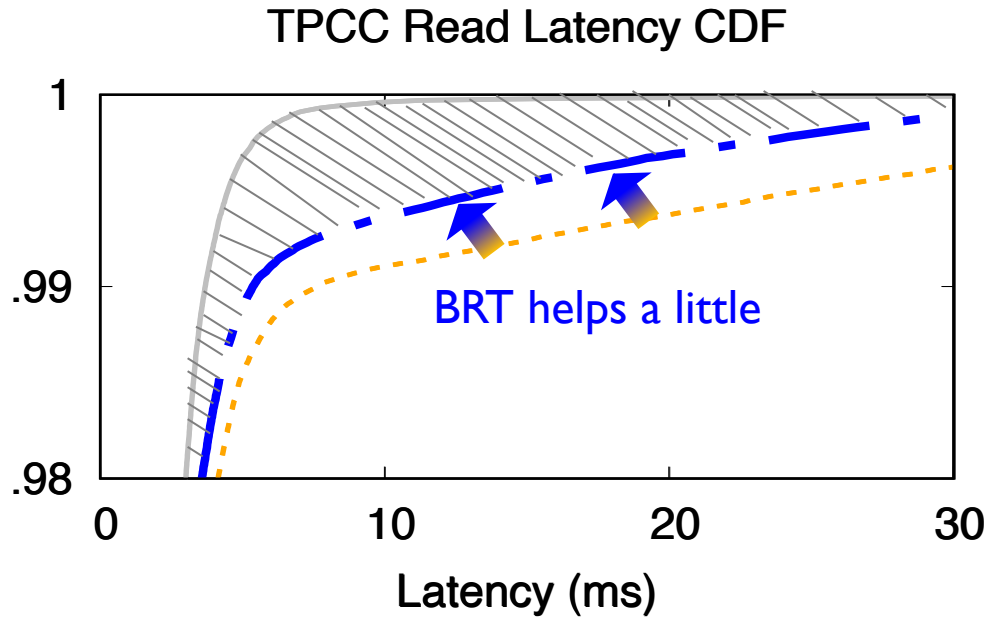


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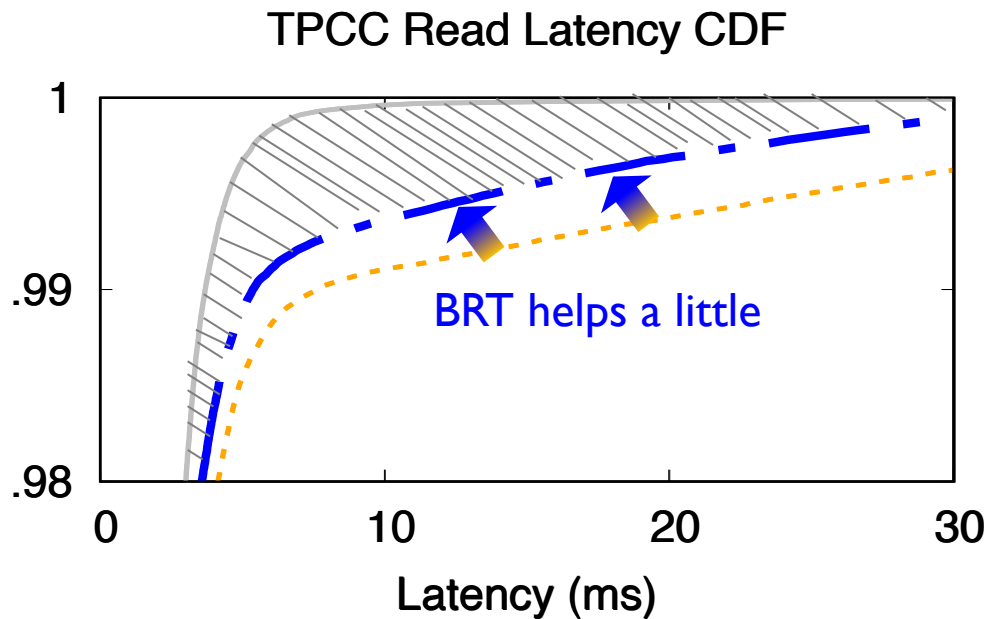




# The Effectiveness of “*BRT*” Interface



# The Effectiveness of “*BRT*” Interface



*Can we do better?*

# IODA Busy Latency Windows



**“Fail-if-Slow”**: the SSD should *fast-fail* an I/O if it contends with GC



**TW Coordination**: SSDs take turns to perform GCs

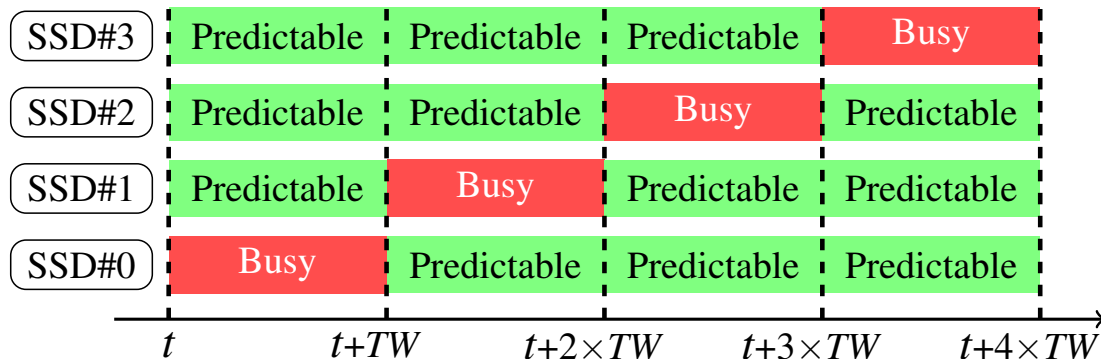
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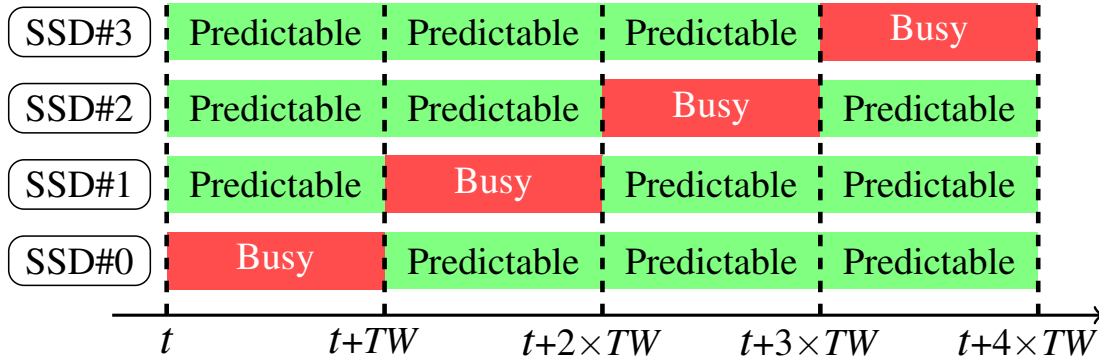


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**IODA: Always Predictable Latencies!**



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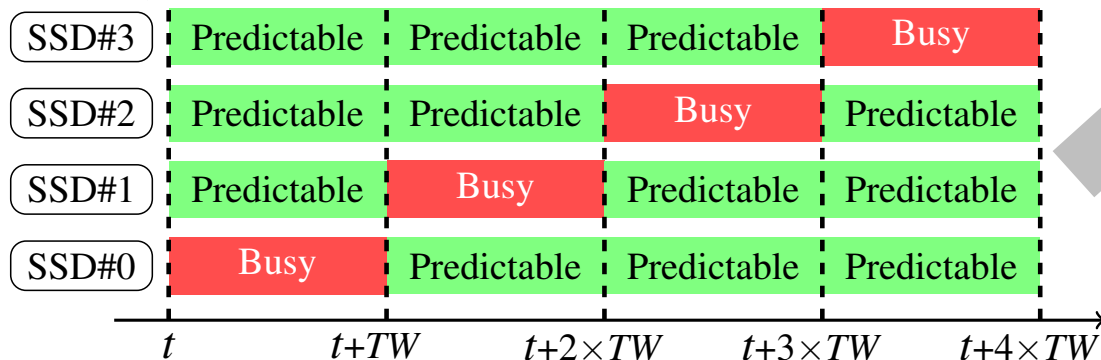


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**TW Coordination**: SSDs take turns to perform GCs

**IODA: Always Predictable Latencies!**



How long should *TW* be?

# IODA Time Window ( $TW$ ) Formulation

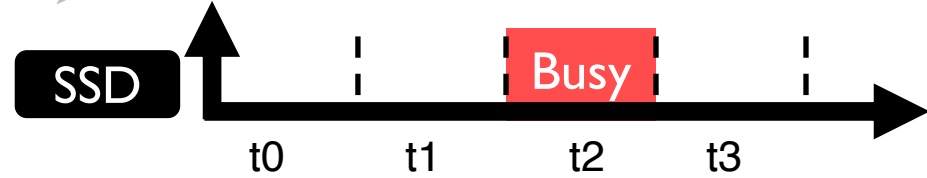
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*SSD free space*  $\geq$  *User load*



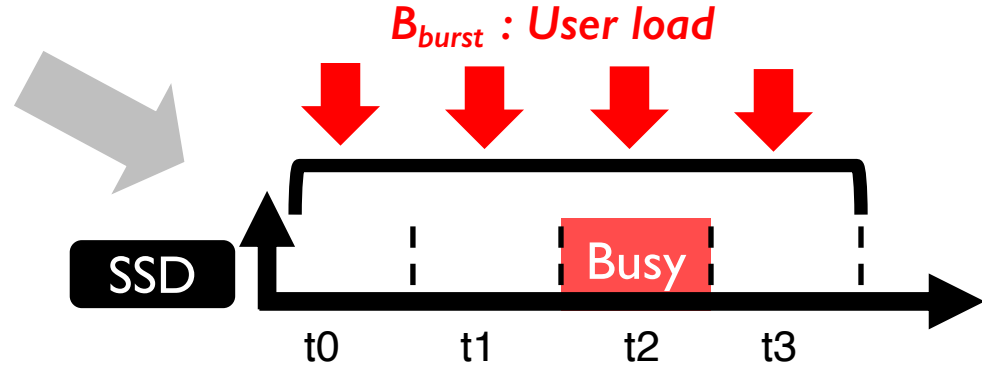
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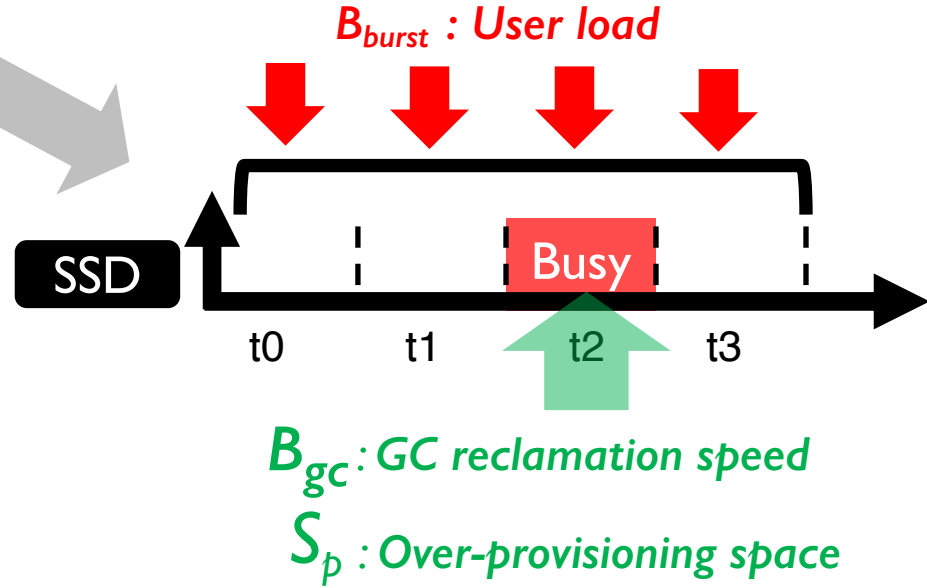
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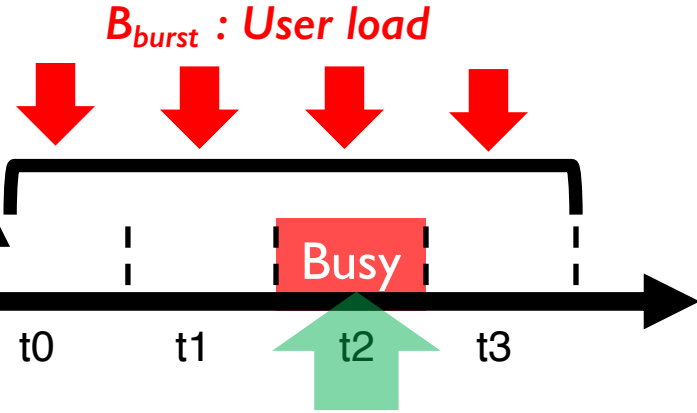


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*SSD free space*  $\geq$  *User load*

$$TW \leq S_p / ((N_{ssd} \times B_{burst}) - B_{gc})$$

SSD



$B_{gc}$  : GC reclamation speed

$S_p$  : Over-provisioning space

# IODA Time Window (TW) Formulation

*SSD free space*  $\geq$  *User load*

$B_{burst}$  : User load

SSD

Busy

t0

t1

t2

t3

$B_{gc}$  : GC reclamation speed

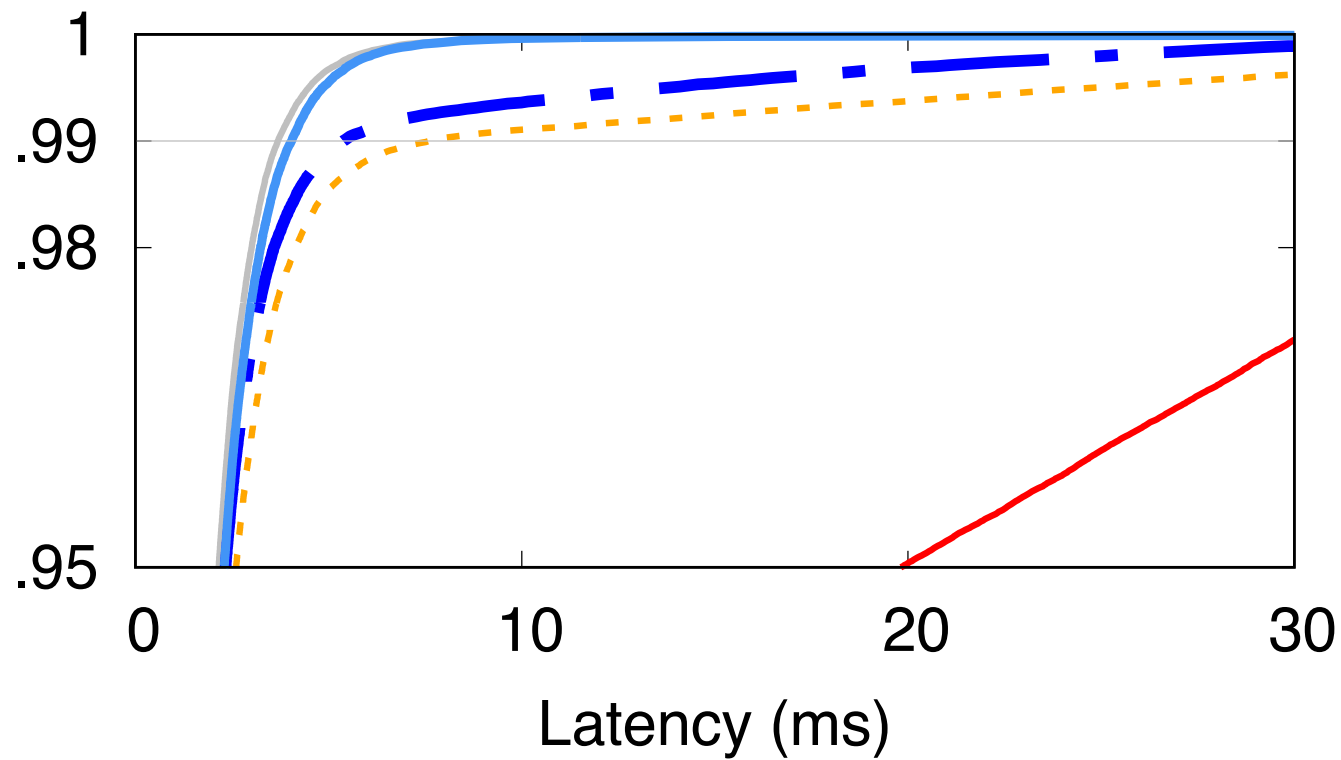
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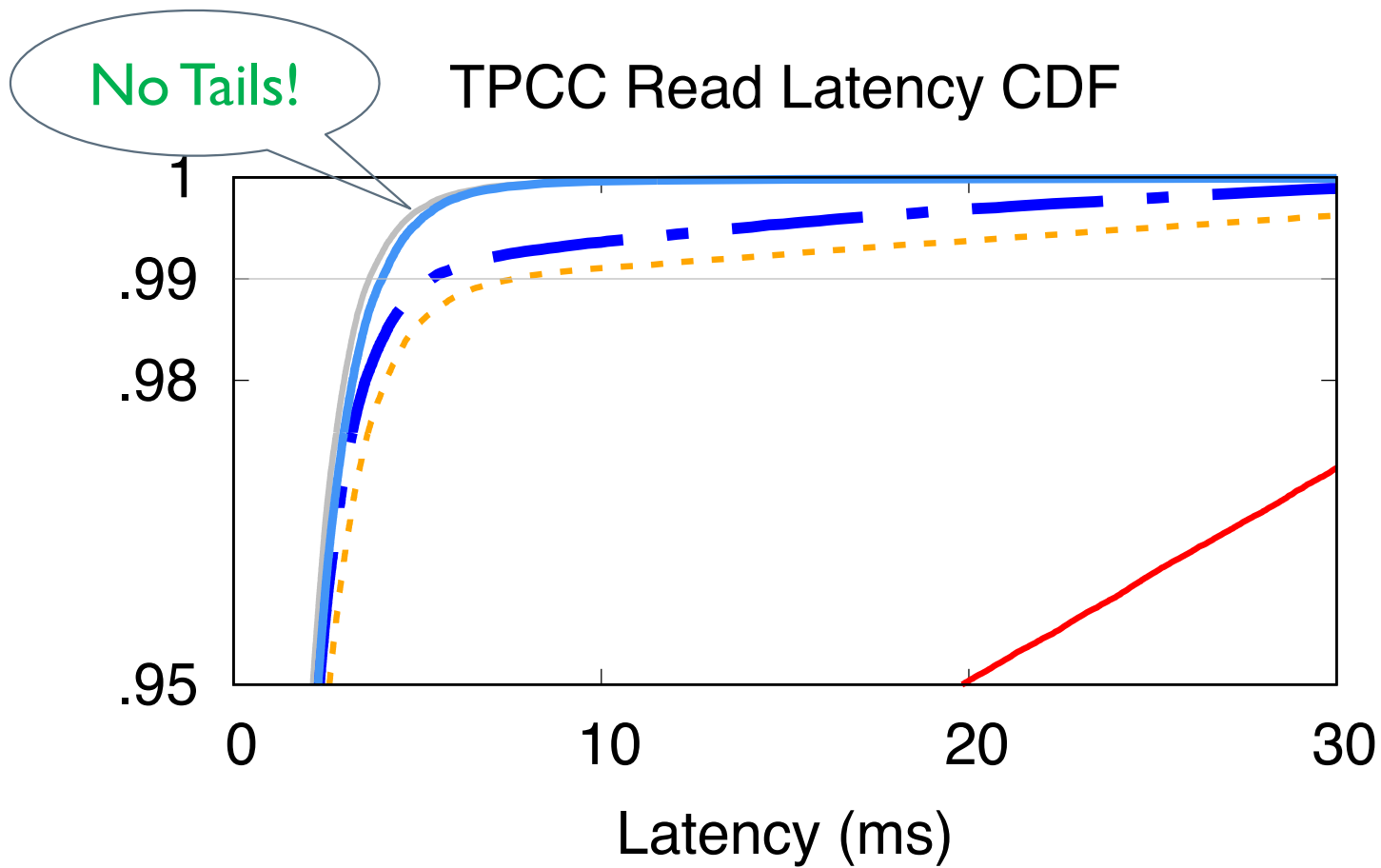
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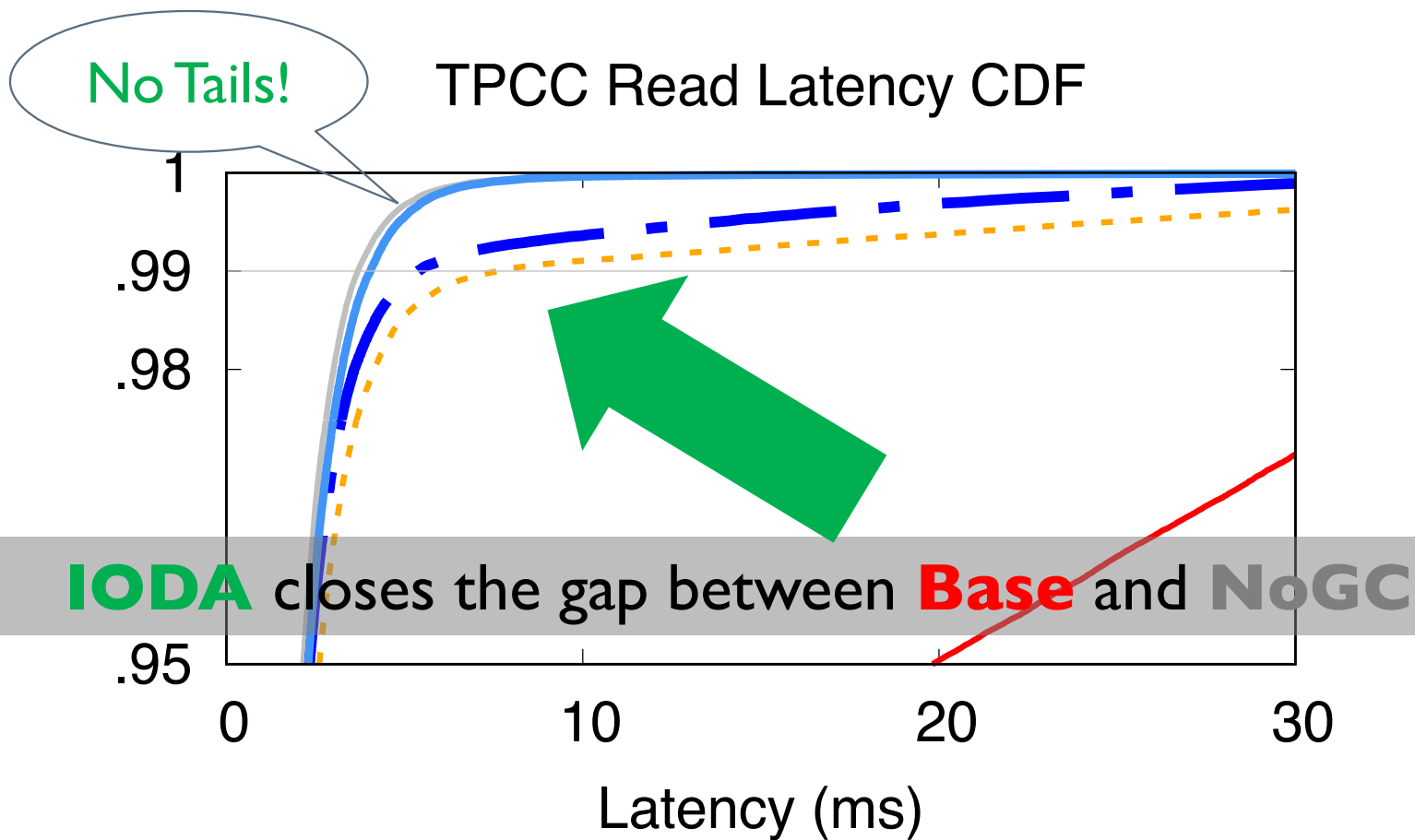
$$TW \leq \frac{R_p \times S_t}{(N_{ssd} \times \text{Min}(B_{pcie}, \text{Max}(\frac{N_{dwpd} \times (1 - R_p) \times S_t}{8\text{hours/day}}))) - (\frac{(1 - R_v) \times N_{ch} \times S_{pg} \times N_{pg}}{(t_r + t_w + 2 \times t_{cpt}) \times R_v \times N_{pg} + t_e})}$$

*TW Upper Bound*

TPCC Read Latency CDF









# More in the paper!

## □ IODA TW analysis

- **6** SSD models
- Relaxed TW
- TW vs. WAF tradeoffs

## □ Implementation

- Platforms: FEMU + OpenChannel-SSD
- Kernel: Linux Software-RAID + NVMe

## □ More evaluation results

- **9** datacenter block traces + **21** real applications
- IODA vs. **7** State-of-the-art approaches
- IODA on OpenChannel-SSD
- IODA throughput and write latency
- ...

### IODA: A Host/Device Co-Design for Strong Predictability Contract on Modern Flash Storage

Huaicheng Li  
University of Chicago and  
Carnegie Mellon University

Martin L. Putra  
University of Chicago

Ronald Shi  
University of Chicago

Xing Lin  
NetApp

Gregory R. Ganger  
Carnegie Mellon University

Haryadi S. Gunawi  
University of Chicago

#### Abstract

*Predictable latency on flash storage is a long-pursued goal, yet, unpredictability arises due to the unavoidable disturbance from many well-known SSD internal activities. To combat this issue, the recent NVMe IO Determination (IOD) interface advocates host-level controls to SSD internal management tasks. While promising, challenges remain on how to exploit it for truly predictable performance.*

*We present IODA, an IO deterministic flash array design built on top of small but powerful extensions to the IOD interface for easy deployment. IODA exploits data redundancy in the context of IOD for a strong latency predictability contract. In IODA, SSDs are expected to quickly fail an IO on purpose to allow predictable I/Os through proactive data reconstruction. In the case of concurrent internal operations, IODA introduces busy remaining time exposure and predictable-latency-window formulation to guarantee predictable data reconstructions. Overall, IODA only adds 4 new fields to the NVMe interface and a small modification in the flash firmware, while keeping most of the complexity in the host OS. Our evaluation shows that IODA improves the 95–99.99<sup>th</sup> latencies by up to 75%. IODA is also the nearest to the ideal, no disturbance case compared to 7 state-of-the-art preemption, suspension, GC coordination, partitioning, stay-sil flash controller, prediction, and proactive approaches.*

#### CCS Concepts

• Computer systems organization → Firmware: Embedded hardware; Embedded software; Information systems → Flash memory; Hardware → Emerging interfaces.

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ACM ISBN 978-1-4503-8780-5/21/09...\$15.00  
<https://doi.org/10.1145/347132.3483973>

#### Keywords

Software/Hardware Co-Design, Predictable Latency, NVMe IO Determination, SSD, Flash Storage

#### ACM Reference Format:

Huaicheng Li, Martin L. Putra, Ronald Shi, Xing Lin, Gregory R. Ganger, and Haryadi S. Gunawi. 2021. IODA: A Host/Device Co-Design for Strong Predictability Contract on Modern Flash Storage. In *ACM SIGOPS 28th Symposium on Operating System Principles (OSPP '21)*, October 26–29, 2021, Virtual Event, Germany. ACM, New York, NY, USA, 17 pages. <https://doi.org/10.1145/347132.3483973>

#### 1 Introduction

Flash arrays are popular storage choices in data centers and they must address users' craving for low and predictable latencies [1–3]. Thus, many recent SSD products are released and evaluated not just on the average speed but the percentile latencies as well [1–7]. These all point the reality that customers would like SSDs with deterministic latencies.

Deterministic latency, however, is hard to achieve because SSD performance is inherently non-deterministic due to the internal management activities such as the garbage collection (GC) process, wear leveling, and internal buffer flush [8–10]. These activities will inevitably trigger many background I/Os and disturb user requests, thereby causing severe latency hiccups. As an illustration, the figure on the right shows the giant latency gap between the “Base” (with GC) and the “Ideal” (no GC) cases. Modern SSDs often resort to large over-provisioning space (e.g., up to 50% of the SSD’s raw NAND capacity [11]) to provide leeway for more efficient background task processing; however, our profiling experiments on recent enterprise SSDs showed that GCs can still cause up to 60% latency increase (details omitted). This is unfortunately still an ongoing problem faced by the storage industry [12–14].  
To tame the SSD performance challenges, there have been many efforts to evolve the device interfaces [15–17]. The Stor-

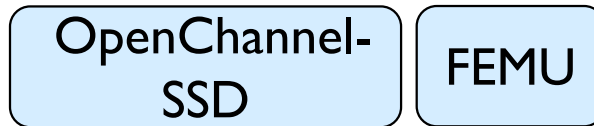


# IODA Stack and Evaluation Setup

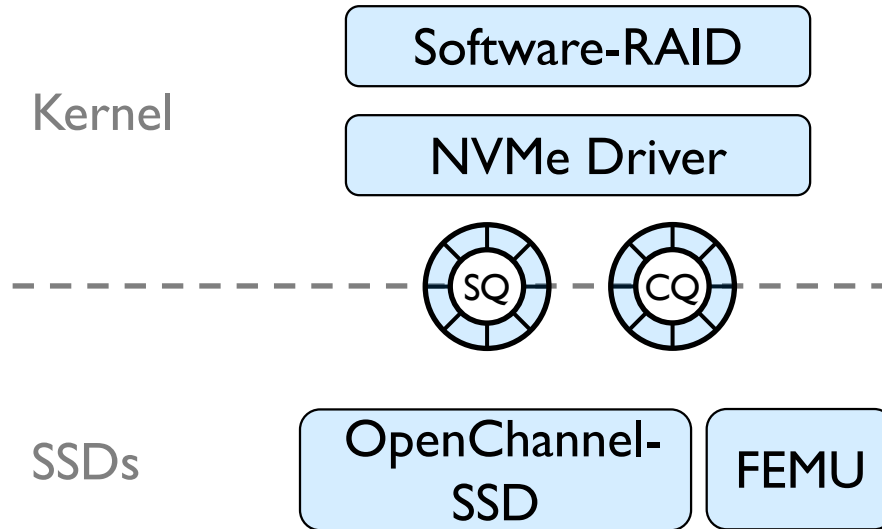
Kernel



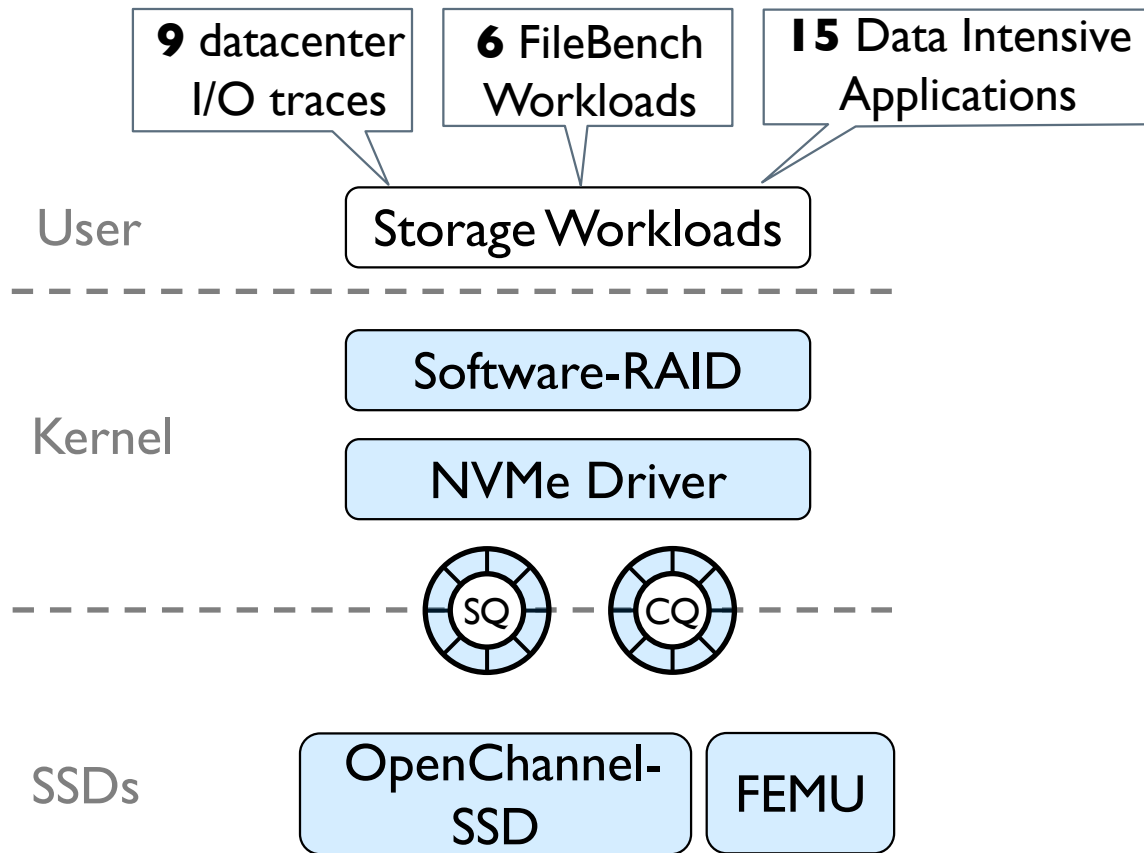
SSDs



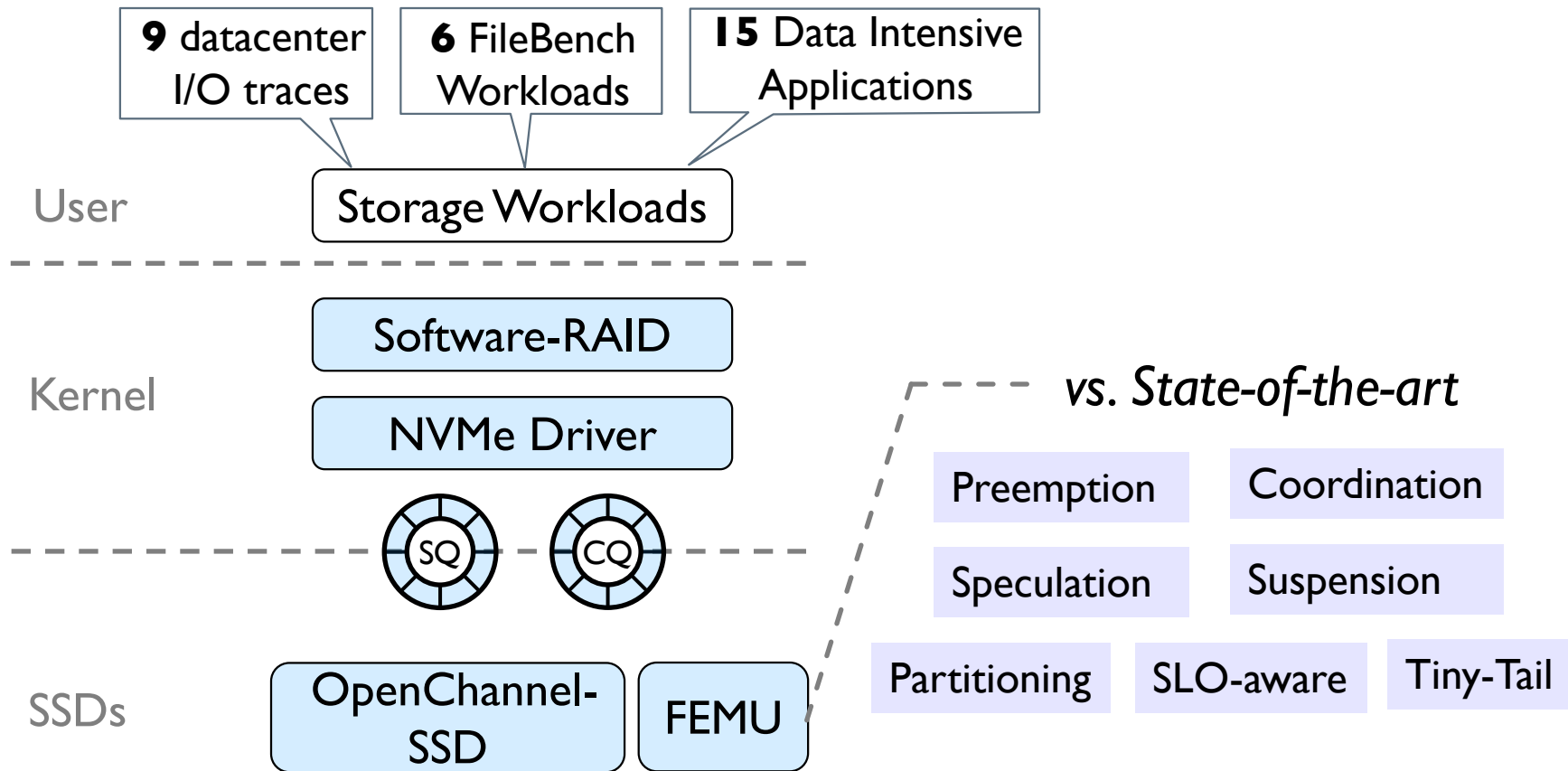
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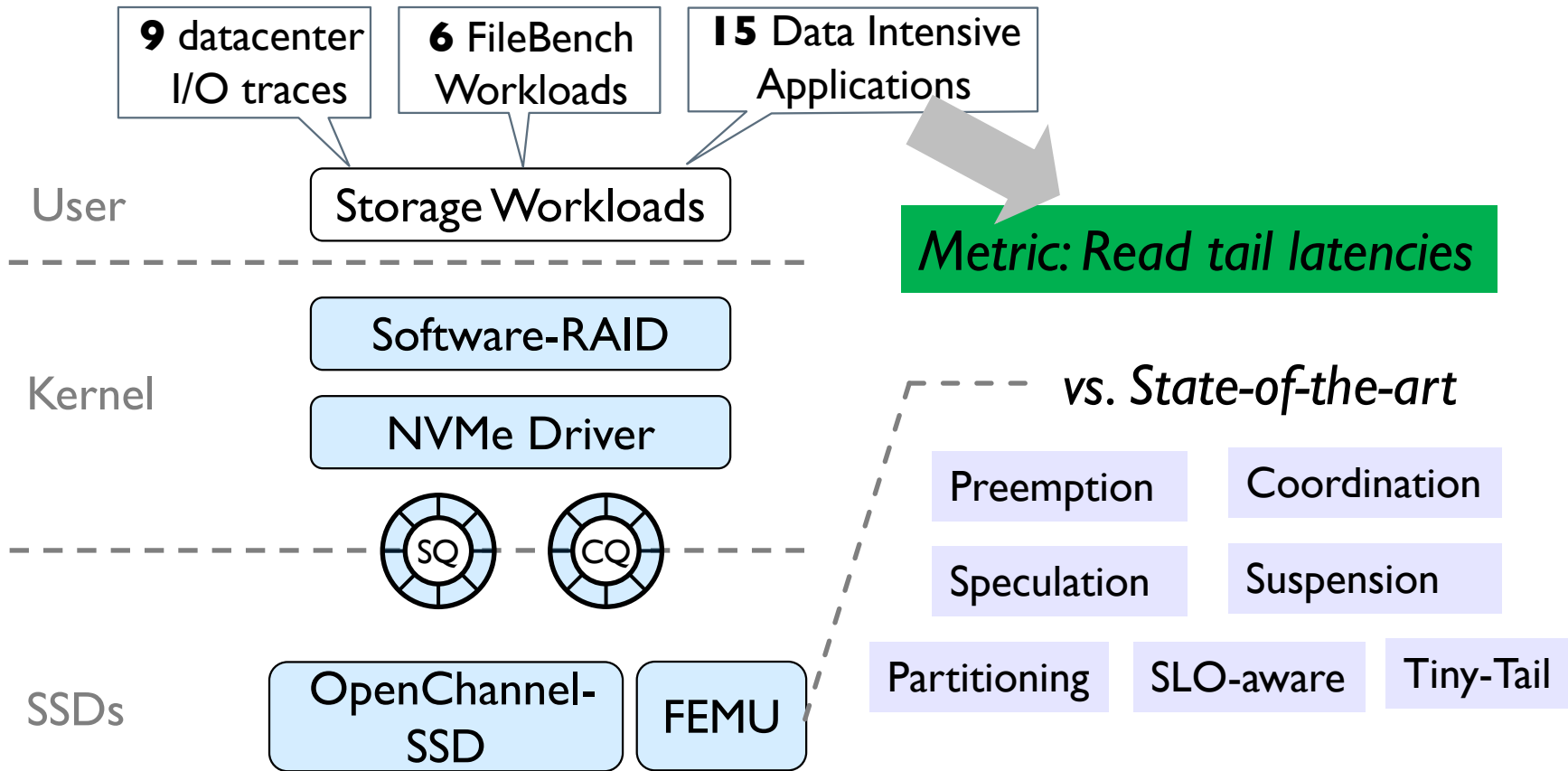
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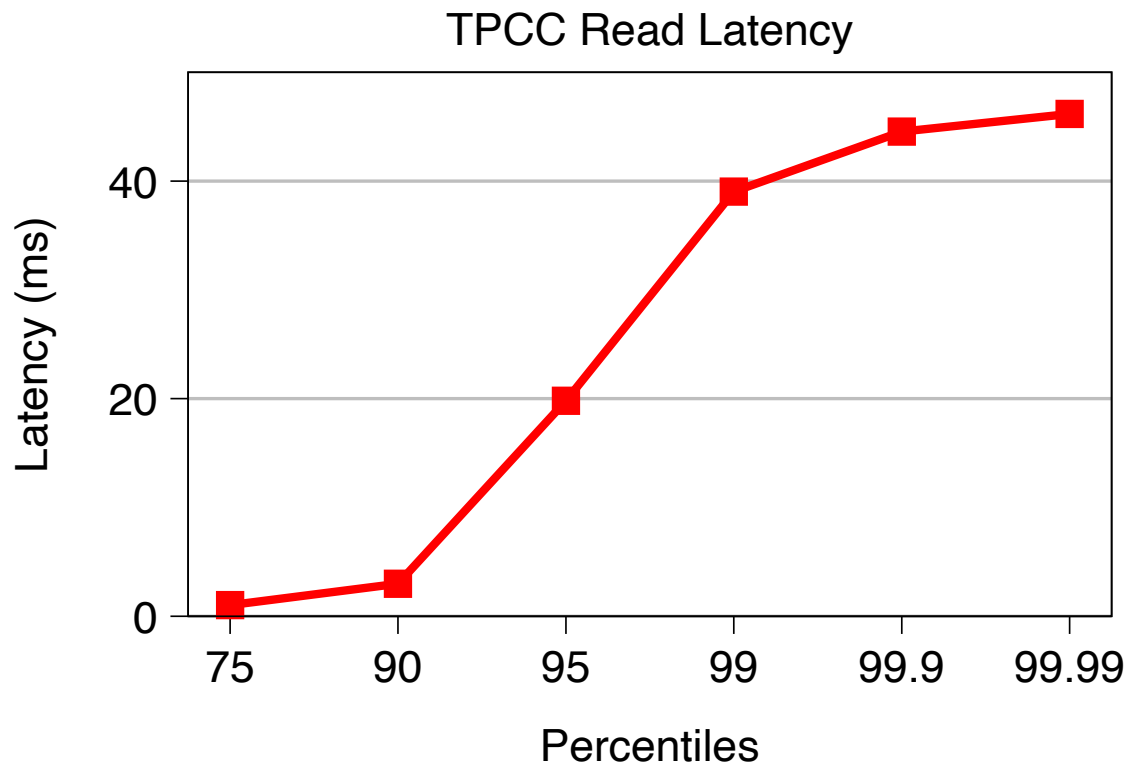
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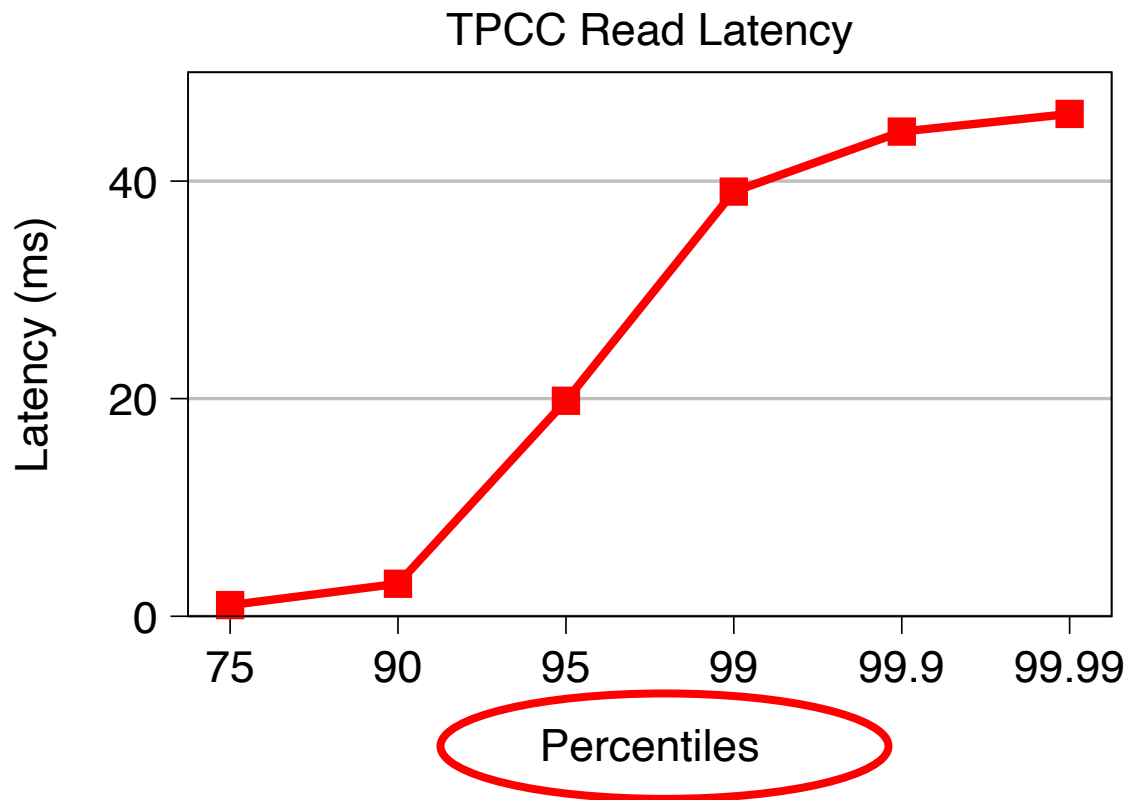
# IODA Stack and Evaluation Setup



# IODA Evaluation



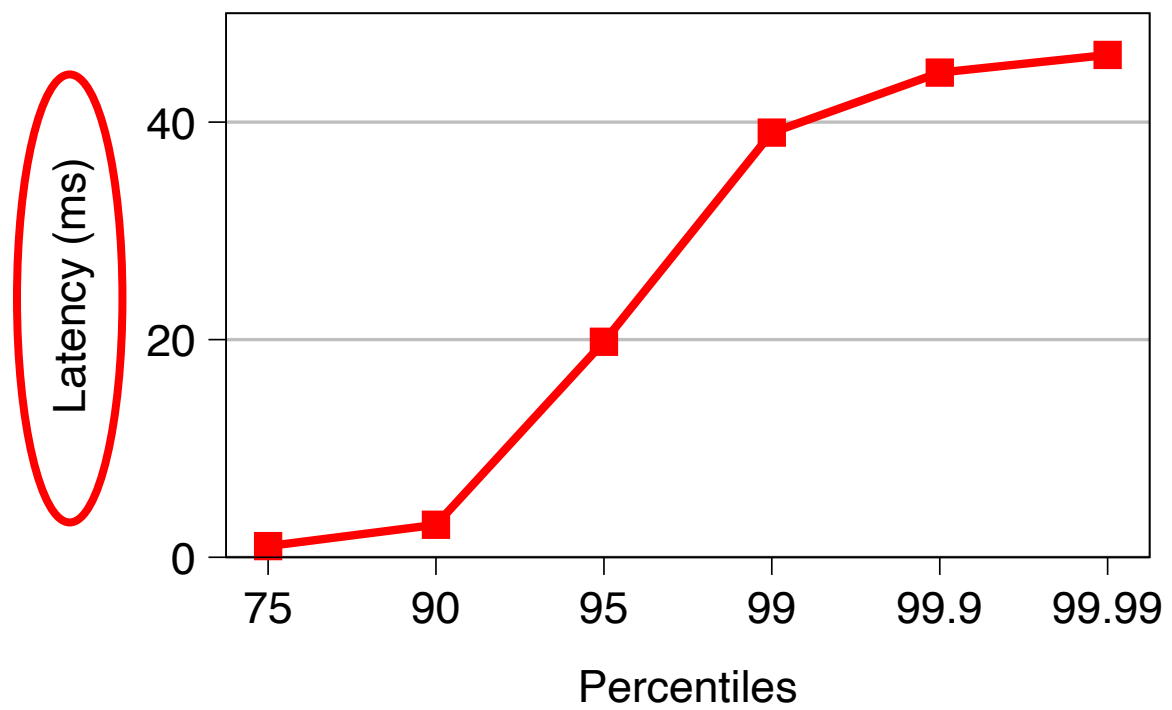
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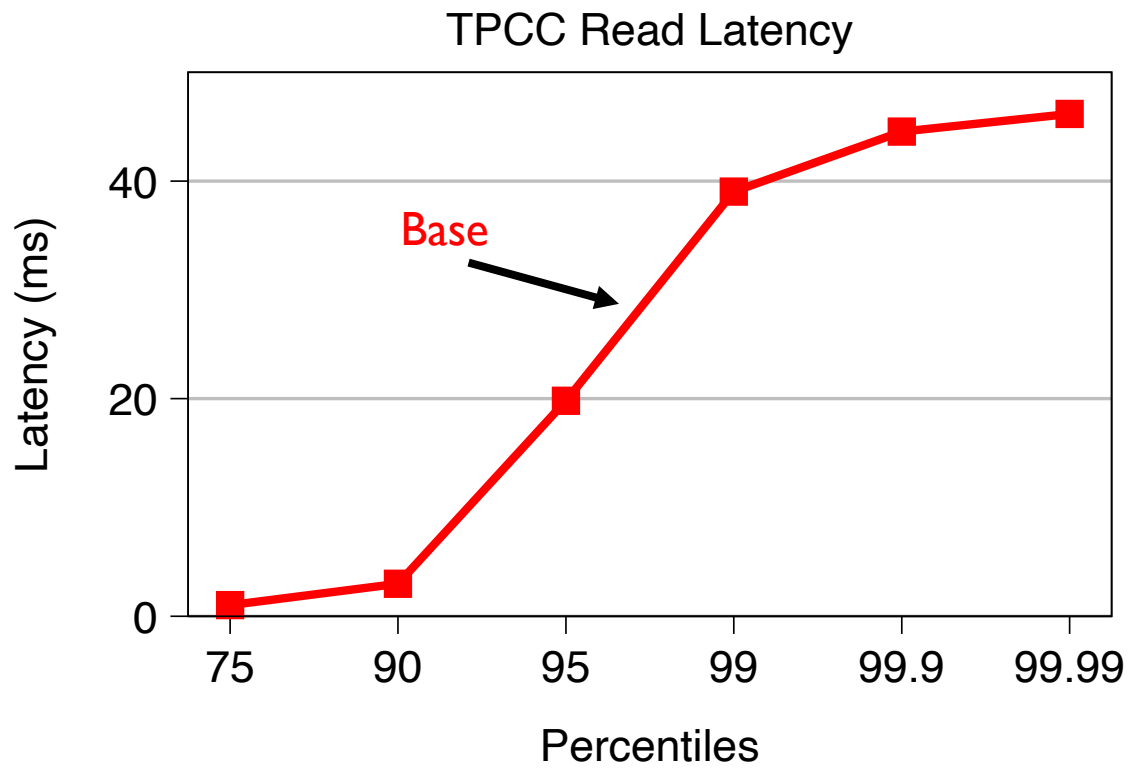


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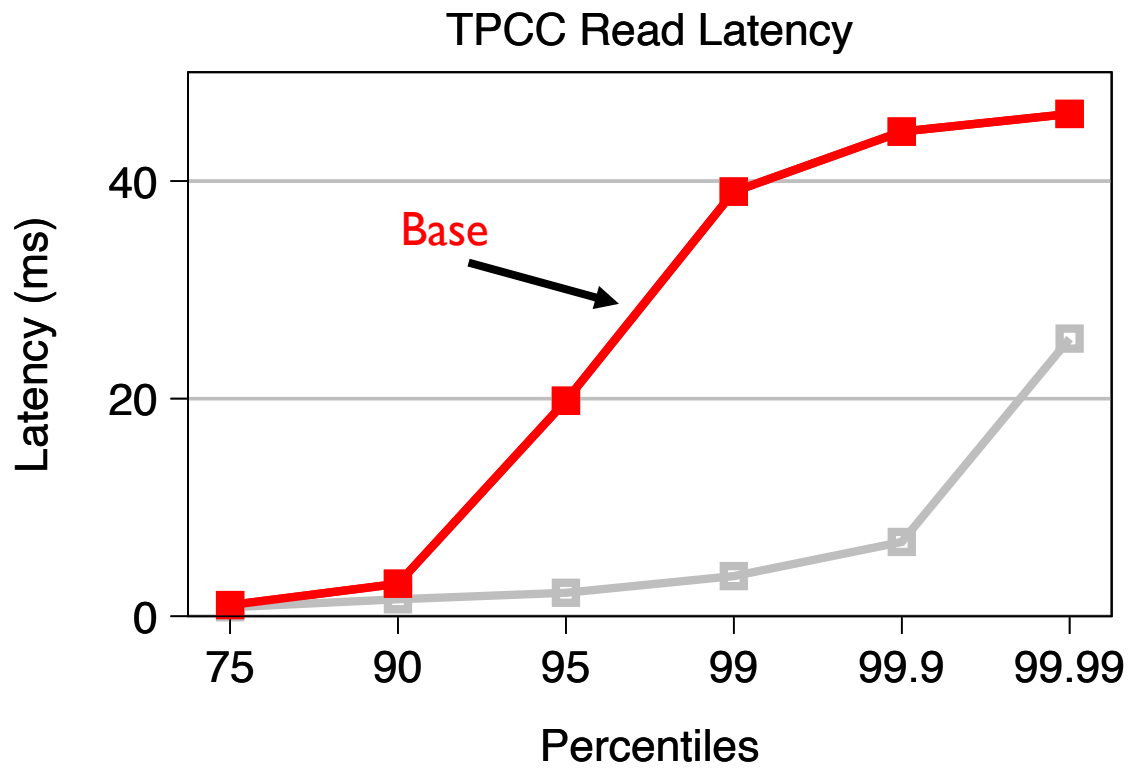
TPCC Read Latency



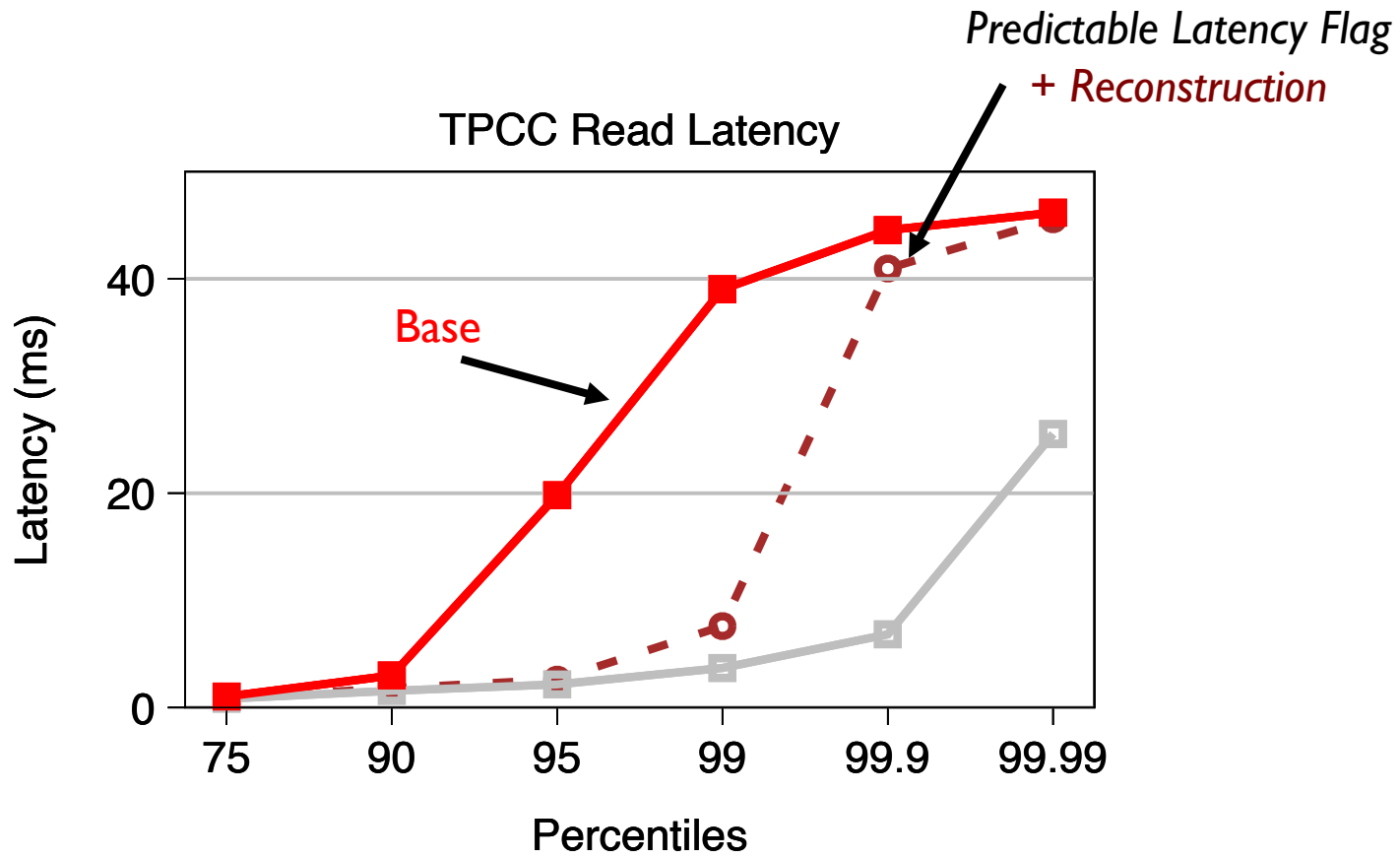
# IODA Evaluation



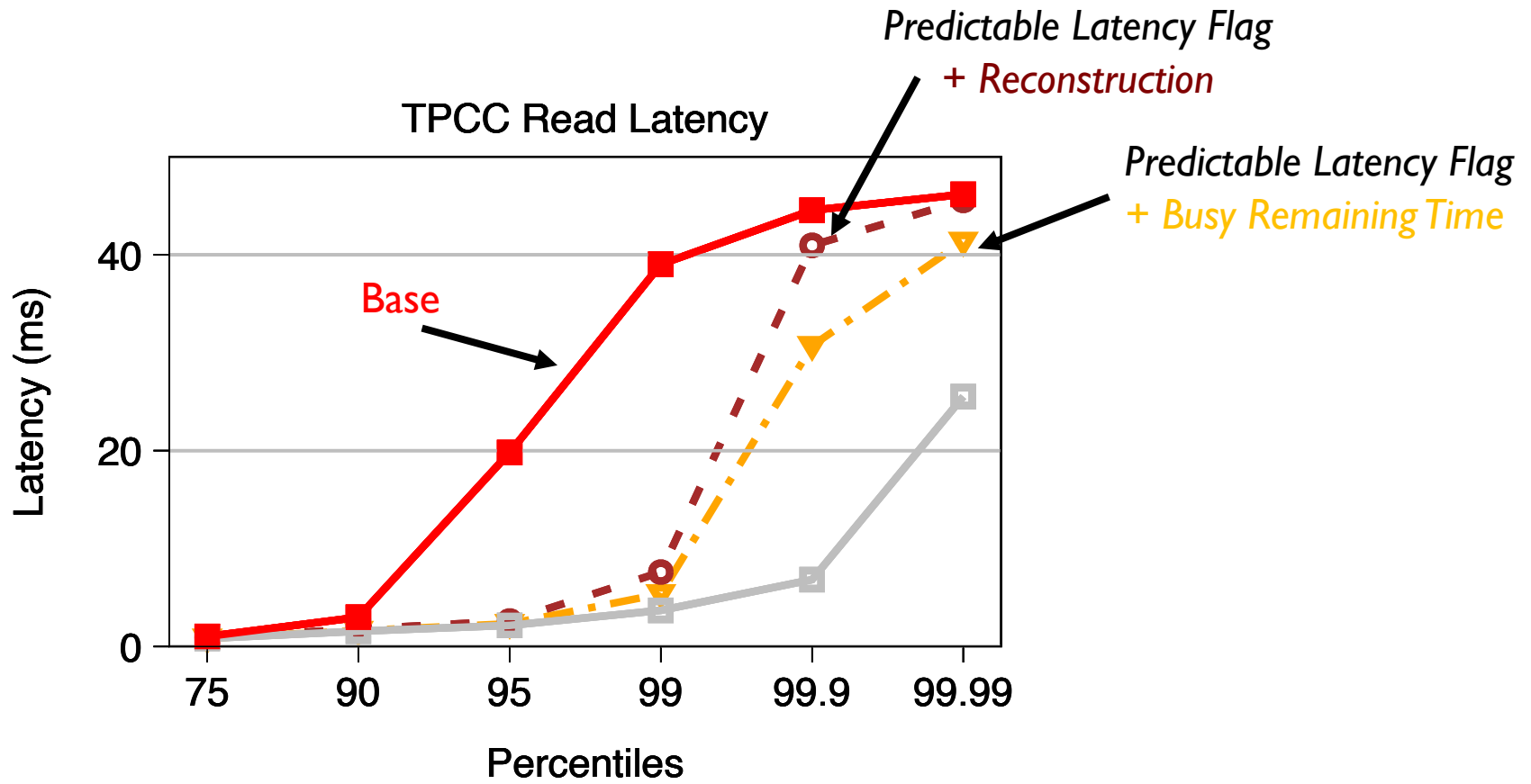
# IODA Evaluation



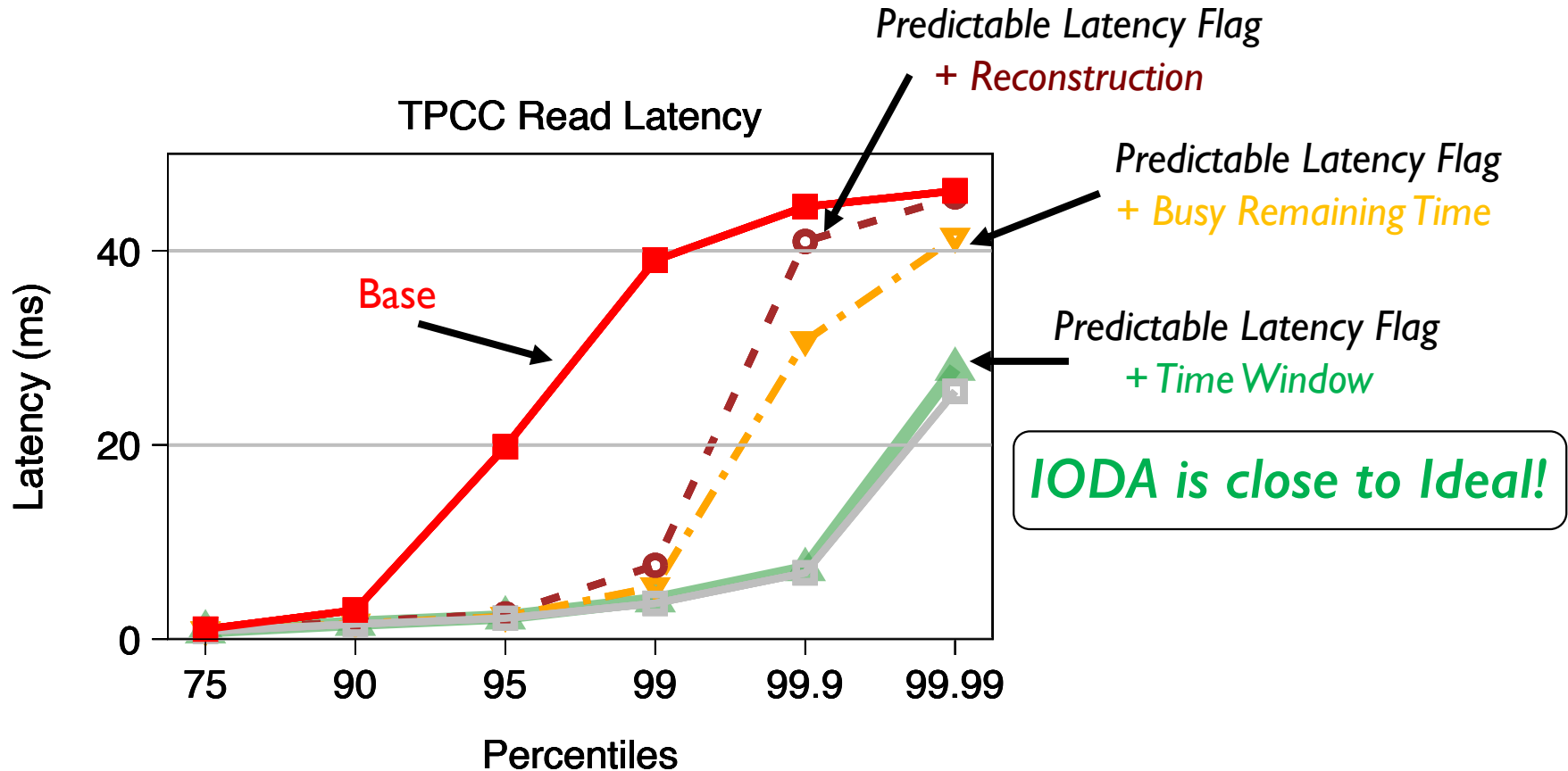
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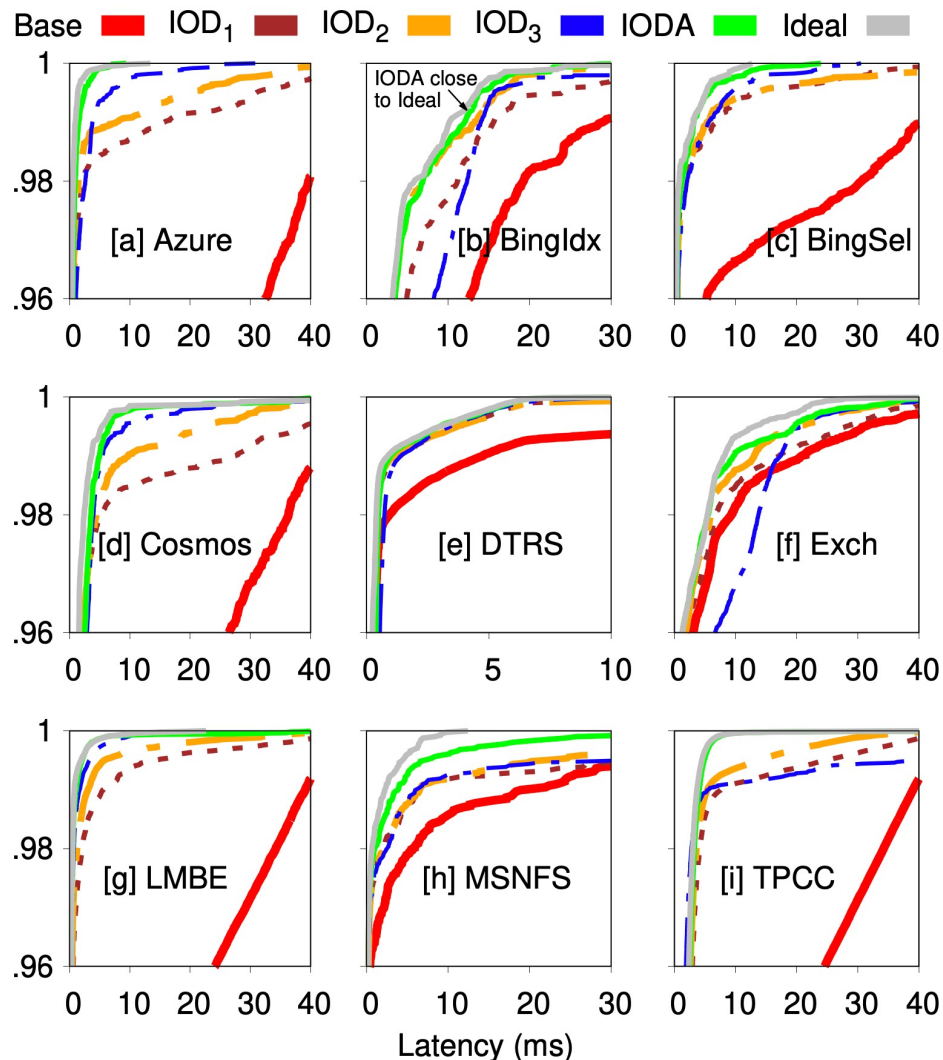


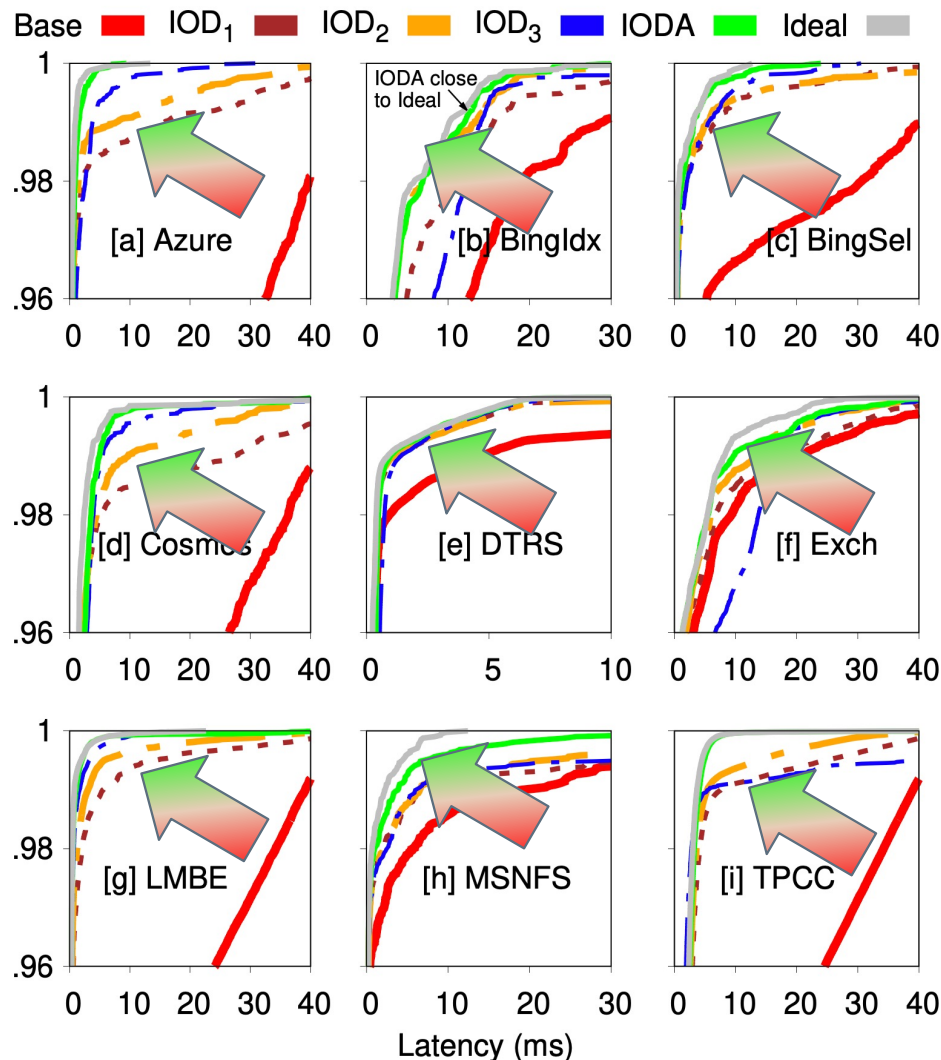
# IODA Evaluation



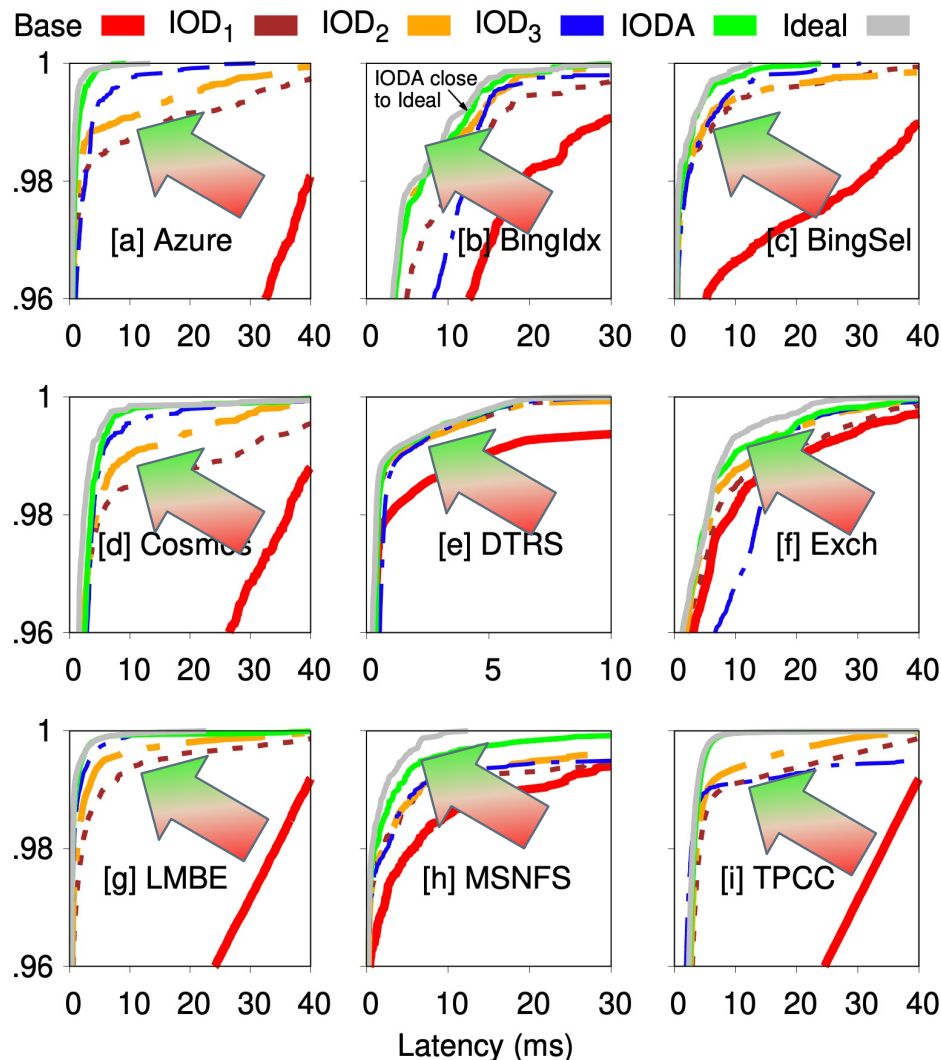
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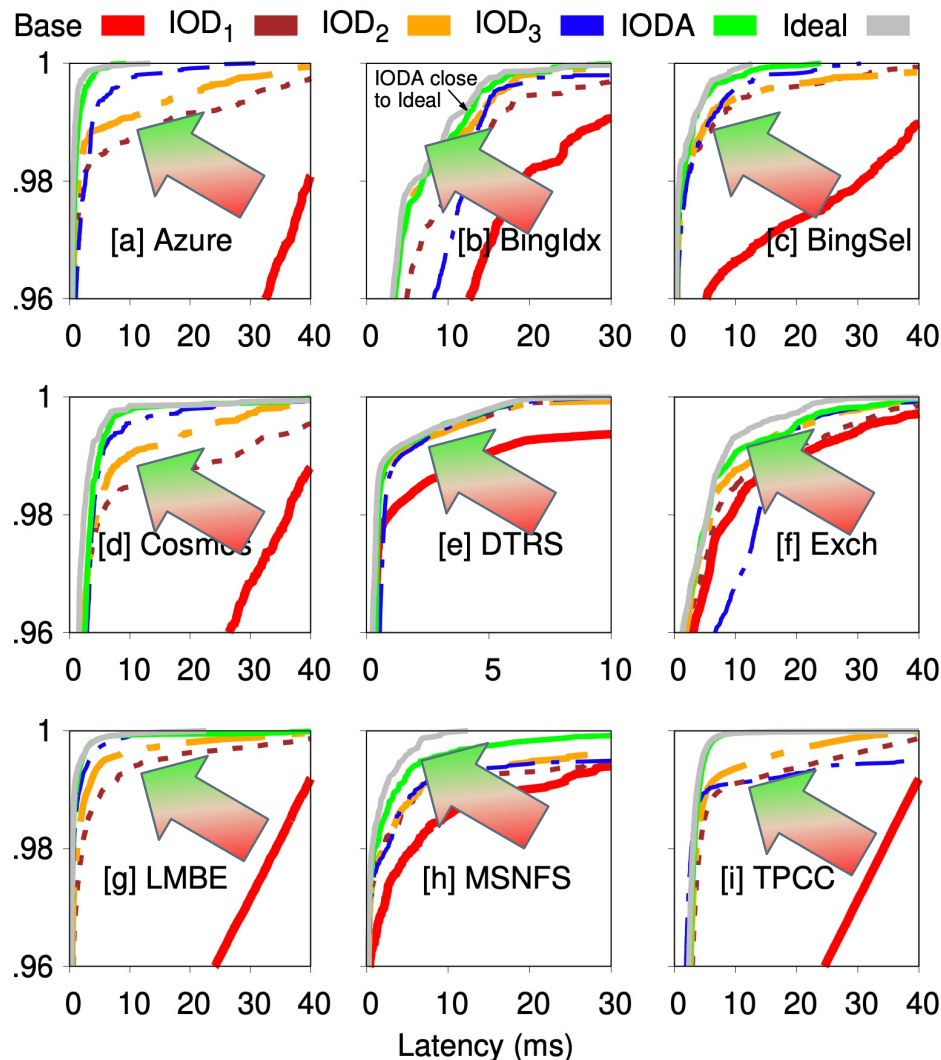








**IODA Results:** (95<sup>th</sup> – 99.99<sup>th</sup>)  
Up to 75x improvement over *Base*



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**VS.**

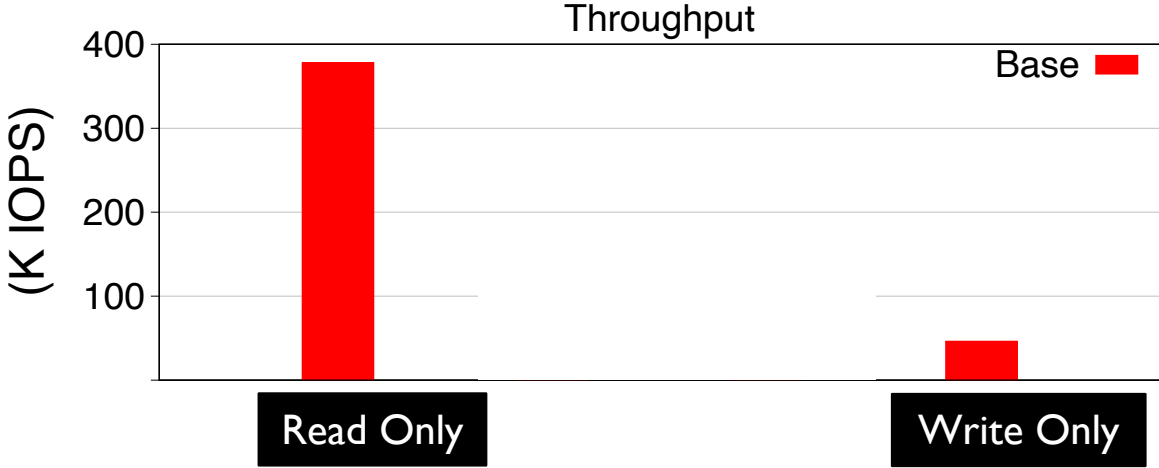
Preemption      Coordination

Speculation      Suspension

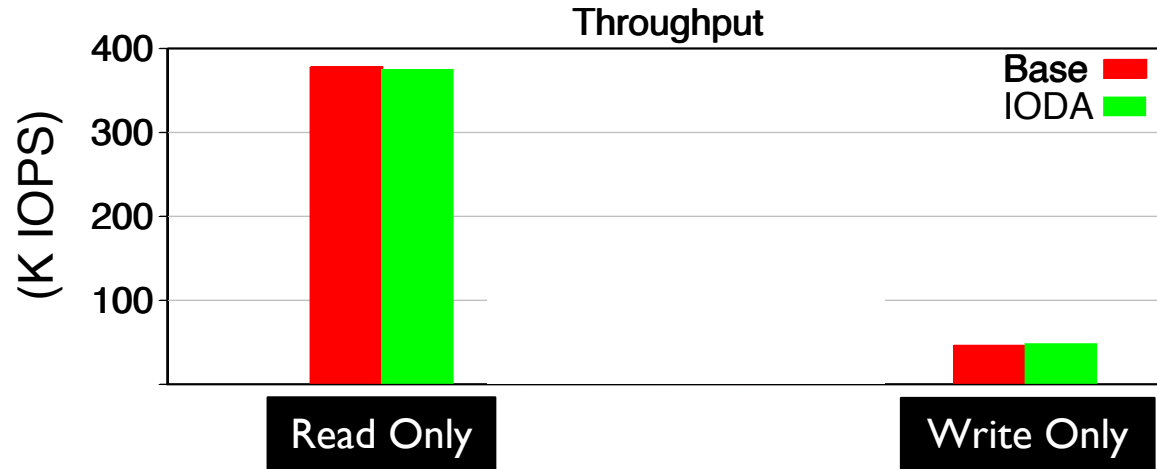
Partitioning      SLO-aware      Tiny-Tail

*IODA is more deterministic and efficient in cutting tail latencies!*

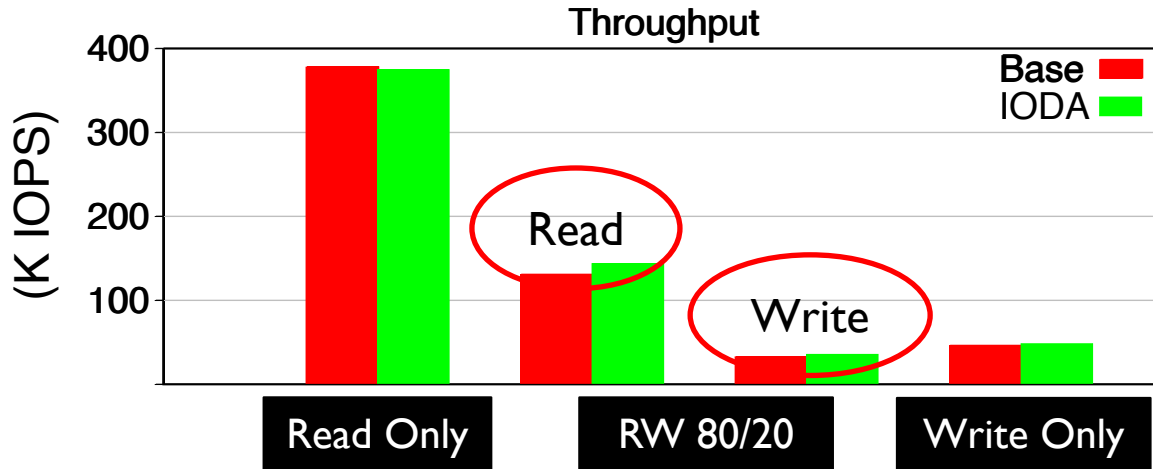
# IODA Throughput



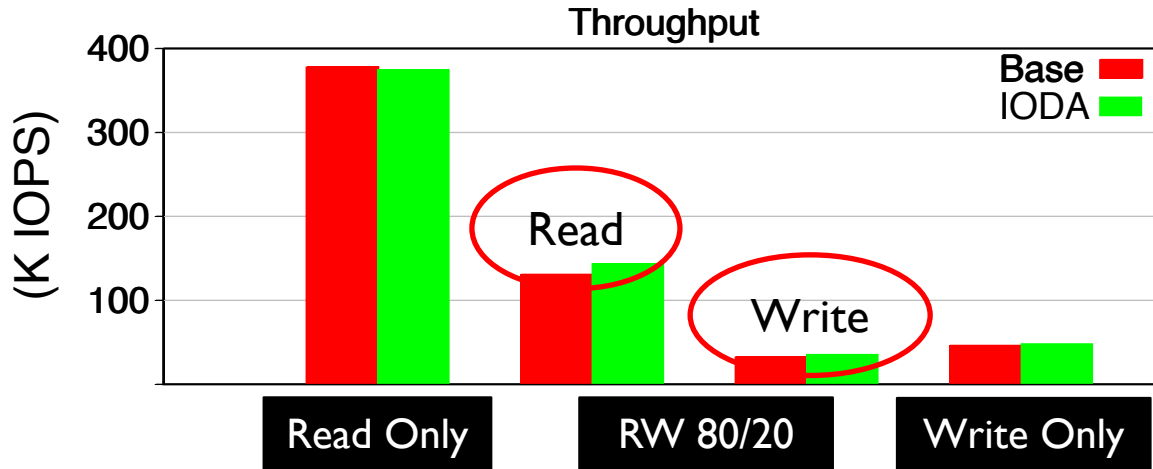
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*IODA doesn't sacrifice the array's aggregate bandwidth*

# IODA Takeaways

- A *Co-Design* Approach for Performance Predictability
  - Proactive *reconstruction* via *fast-fail* interface
  - *BRT* for improved latencies
  - *TW* formulation to program the window length
  - *Cross-device synchronization*

*I'm on the job market.*

IODA: <https://github.com/huaicheng/IODA>

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Thank you!

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