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The Three P's of High-Performance Reconfigurable Computing

Speaker: Prof. Esam El-Araby

The Catholic University of America

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1:00PM- 2:00PM, NVC 207

Abstract

Acceleration of parallel applications using hardware coprocessors has been lately receiving rising attention in both academia and industry. Architectures based on reconfigurable hardware, graphical processors, and multi/many-core processors have been adopted. One example of such architectures is that of the High-Performance Reconfigurable Computers (HPRCs), that are parallel computers but with added FPGA chips as hardware co-processors or accelerators. Examples of such systems are the Cray XD1, the Cray XT5$_h$, the SRC-6, the SRC-7, and the SGI Altix/RASC. HPRCs have potential to provide substantial performance improvements over traditional supercomputers.

In this talk, I will present the historical evolution of HPRC systems, tools, and applications. I will also present solutions from my current and past research work to the challenge trinity or the three P's of HPRCs, i.e. Productivity, Performance, and Portability. For example, I will present an effort to assess HPRC productivity through a review and taxonomy of High-Level Languages (HLLs) and a formal framework for the comparative analysis of their features. Additionally, the performance potential of HPRCs will be demonstrated through a multitude of applications one of which is the problem of numerical non-robustness and exact computations. Finally, a solution based on virtualizing and sharing the reconfigurable resources will be discussed to address the portability challenge.

Biography

Dr. Esam El-Araby joined the Catholic University of America (CUA) as an Assistant Professor in the Department of Electrical Engineering and Computer Science in 2010. He is the founder and director of the HEterogeneous and Biologically-inspired Architectures (HEBA) laboratory at CUA. Prior to that, he worked at the High Performance Computing Laboratory (HPCL) at GWU as well as the NSF Center for High-Performance Reconfigurable Computing (NSF-CHREC). His research work was mainly funded by organizations such as DoD, DARPA, NSF, and NASA and was published in national and international gatherings organized by IEEE, ACM, and NASA. His publication record includes two book chapters on High-Performance Reconfigurable Computing (HPRC) systems and remote sensing, 12 journal papers, and 47 conference papers. His research interests include computer architecture, hybrid/heterogeneous architectures, hardware acceleration, reconfigurable computing, embedded systems, evolvable hardware, performance evaluation, and applications of HPC to digital signal/image processing and remote sensing.